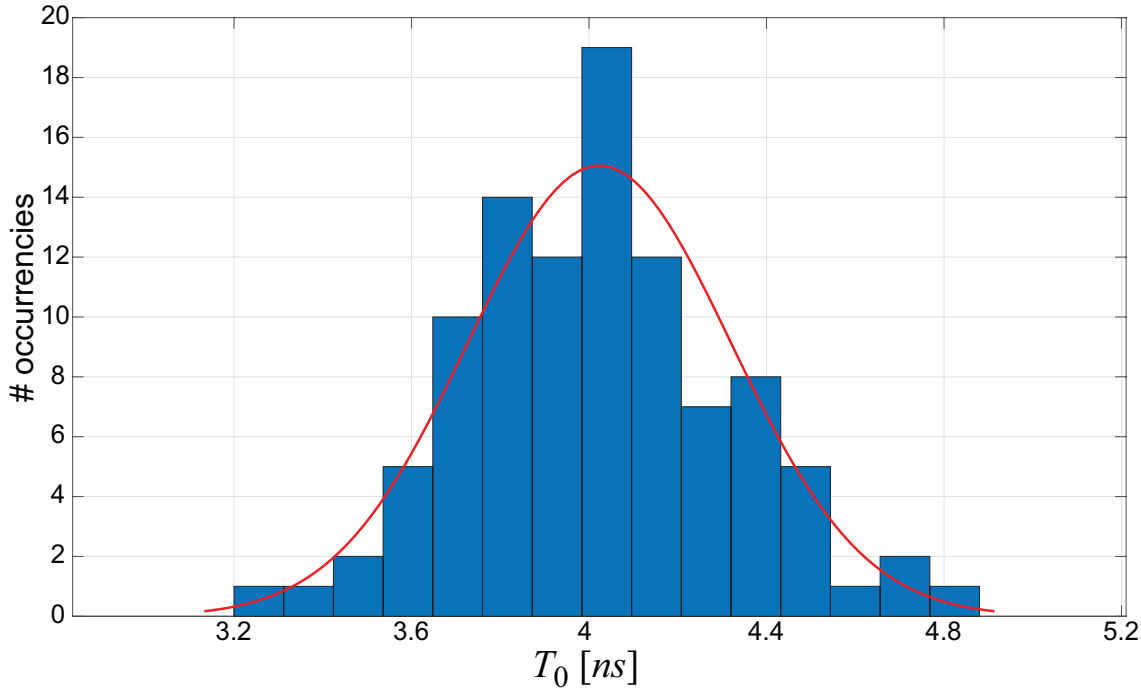

Figure 4.10: The period distribution obtained with 100 Monte Carlo simulations, with a standard 3σ perturbation of the UMC 180 nm technological process parameters and transistors mismatching.

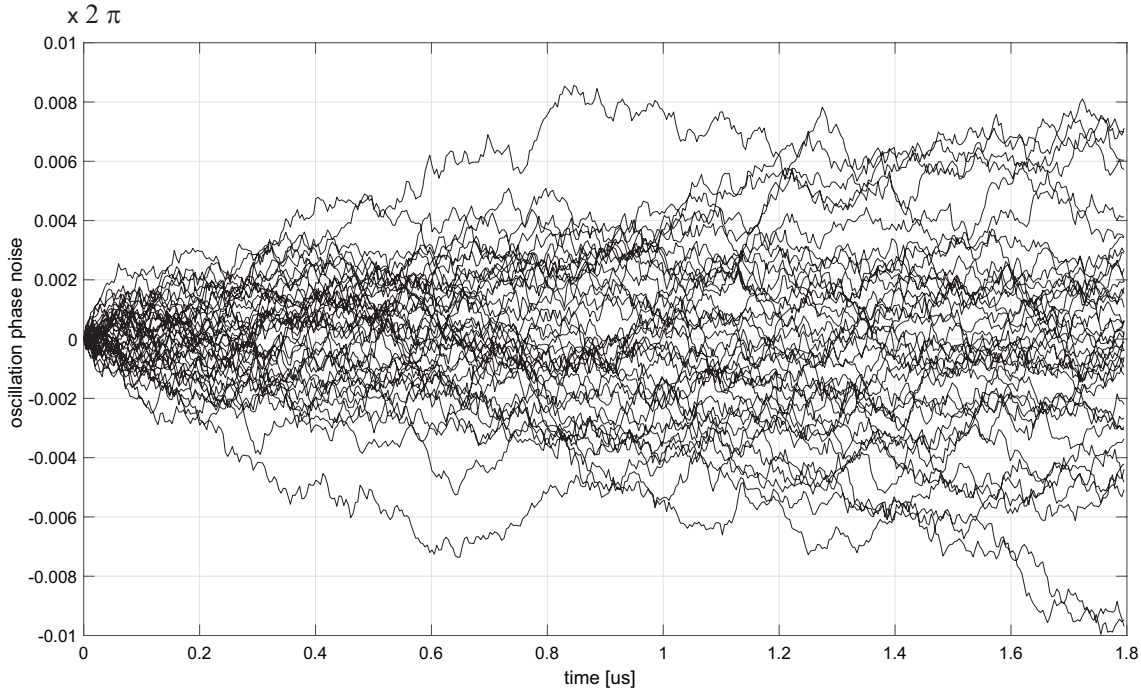

Figure 4.11: Oscillation phase noise of the oscillator with excitation signal turned off, evaluated with 100 Monte Carlo simulations in presence of a moderate electronic noise.

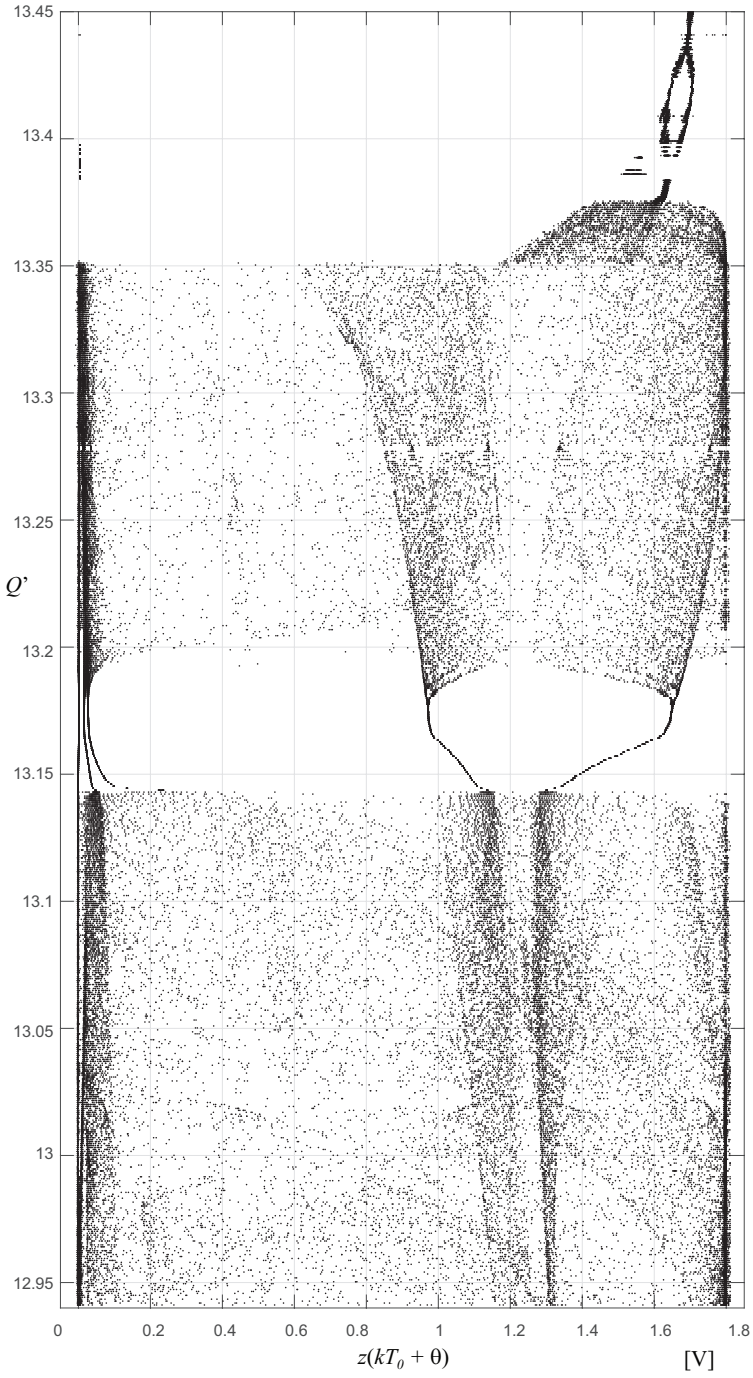

Figure 4.12: Bifurcation diagram obtained by simulating the circuit in Fig. 4.8, reporting the set $\{z(t_k) \in [0V, 1.8V], t_k = kT_0 + \theta, 100 < k < 200\}$, for $\theta = 30\,\text{deg}$, setting the same initial condition in all cases.

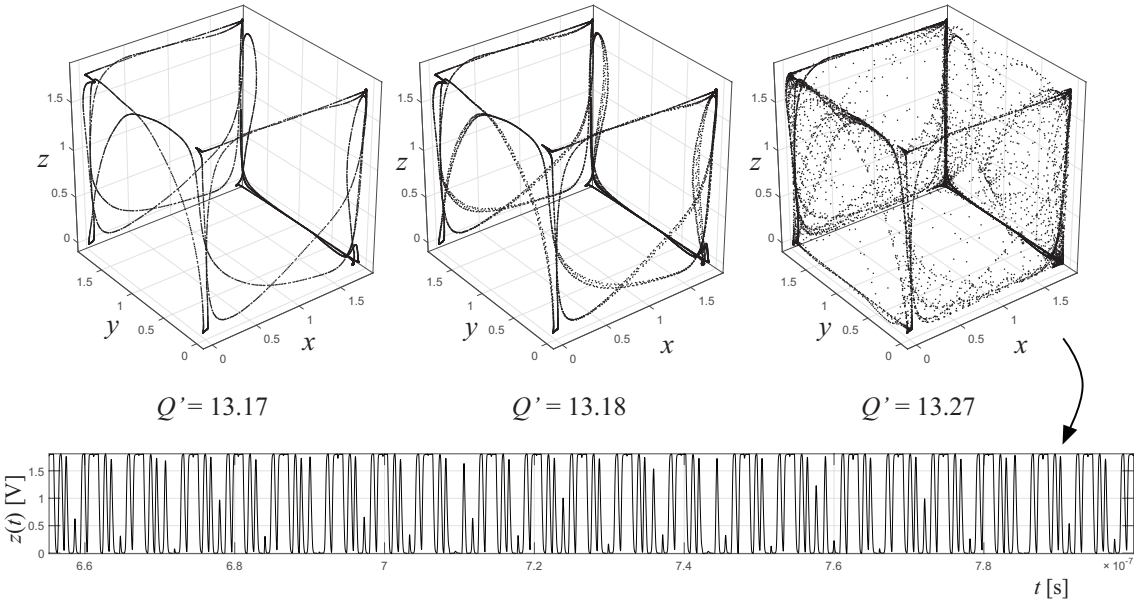

Figure 4.13: Three cases showing period-doubling for $Q' = 13.17, 13.18$ and chaos for $Q' = 13.27$ in the 3D-projections of the voltages x, y, z in Fig. 4.8. For the last chaotic case, the transient simulation of the signal z is reported.

posed of the XOR and the NXOR do not include the DEL delay blocks. In practice, these blocks were implicitly integrated in the connections between gates (the green elements in the figure), assuming that each connection must pass through active routing elements (the white elements in the figure), as it happens inside a PLD.

The circuit proposed in Fig. 4.14 offers interesting design challenges. The ratio between the frequency of the Ring Oscillator and the natural frequency of the controlled oscillator can be changed by varying the number of nodes that make up the three loops of the topology. However, the simulations performed on the circuit (including Monte Carlo analysis) show that there are also other important aspects that can affect the dynamics of the system. In particular:

- given the nominal circuit design, mismatches between transistors, process variability, and other implementation outcomes beyond the designer control (such as delays in the switch matrices involved in routing) can produce different complex dynamics, including chaos; for clarity, Fig. 4.15 shows two example simulations performed on the same nominal circuit but with different mismatches;

- given any simulated hardware implementation, multiple attracting ω-limit sets can coexist, partitioning the phase state of the system into disjoint attraction basins linked to different dynamical behaviors;

- given a simulated hardware implementation, if we add noise to the simulation, it is possible that switching between different attracting ω-limit sets occurs.

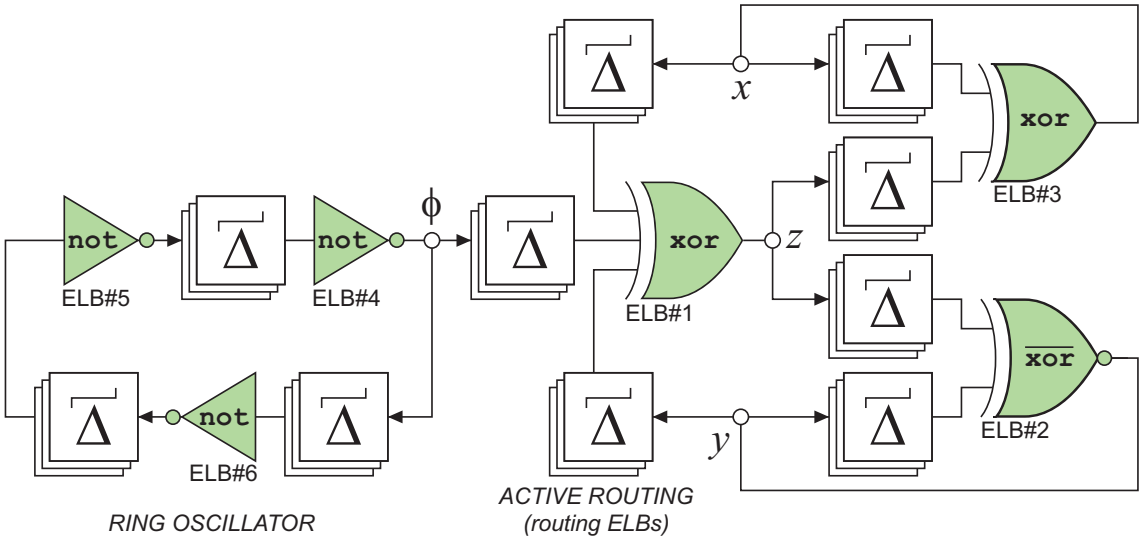

Figure 4.14: The complete topology, in which a nonlinear oscillating structure (the nonlinear oscillator in Fig.4.8), is excited by a Ring Oscillator to produce complex dynamics. The green elements are the nodes of the DNO, the white elements are digital delays representing the active routing elements of a PLD.

All this implies that the dynamics resulting from a certain implementation is highly sensitive to relevant aspects that are not under the control of the designer.

4.5 Implementation

Once the advanced simulation phase of the topology is completed, to conclude the analysis of the DNO we must validate the obtained results through its FPGA implementation.

To assess the topology performance, we compared the circuit in Fig. 4.14 (DNO C) with two other reference DNOs, namely a 7-nodes Ring Oscillator (Fig. 4.16, DNO A), and a 7-nodes Galois Ring Oscillator (Fig. 4.16, DNO B). We selected these oscillators because:

- they have a hardware complexity similar to DNO C;
- both exhibit stable periodic dynamics, DNO A simple and DNO B more complex;
- in both, the information generation mechanism is due to phase noise and jitter caused by electronic noise.

All three circuits were designed by description in VHDL language, following the design rules described in Section 3.5.

Going into more detail, the DNOs were designed on Xilinx Artix 7 xc7a35 FPGAs, with a clock frequency of 100 MHz. For each topology, 16 instances were