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Complex Dynamics in Digital Nonlinear Oscillators: Experimental Analysis and Verification

Tommaso Addabbo, Ada Fort, Riccardo Moretti *, Filippo Spinelli and Valerio Vignoli

Department of Information Engineering and Mathematics, University of Siena, 53100 Siena, Italy; tommaso.addabbo@unisi.it (T.A.); ada.fort@unisi.it (A.F.); filippo.spinelli@student.unisi.it (F.S.); valerio.vignoli@unisi.it (V.V.)

* Correspondence: riccardo.moretti@unisi.it

Abstract: A specific topology of Digital Nonlinear Oscillators (DNOs) has been implemented by using commercial off-the-shelf digital components to experimentally verify and demonstrate the capability of these circuits to support complex dynamics, independently from their implementation technology. In detail, a direct experimental evidence of the DNO dynamical behavior is presented at the analog level with a bifurcation diagram analysis, investigation of periodic and chaotic attractors, and dynamical stability. The autonomous circuit has been investigated as a source of entropy, adopting different figures of merit, including the Lempel–Ziv Complexity, to evaluate the dynamics measured under different operating conditions.

Keywords: digital nonlinear oscillators; nonlinear dynamical systems; chaotic circuits; complex dynamics

Citation: Addabbo, T.; Fort, A.; Moretti, R.; Spinelli, F.; Vignoli, V. Complex Dynamics in Digital Nonlinear Oscillators: Experimental Analysis and Verification. *Electronics* **2023**, *12*, 2459. https://doi.org/10.3390/electronics12112459

Academic Editors: Abdelali El Aroudi, Costas Psychalinos, Esteban Tlelo-Cuautle and Ahmed S. Elwakil

Received: 29 April 2023
Revised: 27 May 2023
Accepted: 27 May 2023
Published: 30 May 2023

1. Introduction

A new class of circuits named Digital Nonlinear Oscillators (DNOs) has been recently proposed for the design of fully digital True Random Number Generators (TRNGs). As defined in [1], DNOs are networks of electronic digital circuits designed to behave as asynchronous logic gates, implementing autonomous nonlinear dynamical systems exhibiting oscillations in the time-continuous domain.

Different full-digital oscillating asynchronous circuits presented in the literature can be viewed as DNOs. These range from the well-known ring oscillator to the more complex Fibonacci and Galois ring oscillators proposed by Golíc in 2006 [2]. Inspired by the circuit topologies of synchronous Linear Feedback Shift Registers (LFSRs), in the structures proposed by Golíc, the synchronous registers are substituted with digital inverters, act as delay elements, and obtain networks of inverting gates with multiple XOR-ed feedbacks. A number of full-digital random number generators have been investigated in the literature, exploiting entropy sources based on these asynchronous circuits [3–15].

In [1], it has been suggested that proper combinations of low-complexity digital primitives can define dynamical system models *supporting structurally stable chaotic dynamics*. More in detail, in previous works, the authors investigated DNOs by means of low-complexity nonlinear dynamical models, circuit simulations, and experimentally, by implementing low-complexity architectures in FPGAs [1,3,5,14]. In the latter experiment, evidence about time-continuous complex dynamics could be presented resorting to indirect measurements and investigating binary sequences obtained through one-bit sampling at different sampling rates, depending on the FPGA master clock. However, this setup did not allow tracking and monitoring of the electrical dynamics at an analog level, making it impossible to investigate numerous aspects related to the dynamics of the nonlinear circuit, such as the analysis of experimental bifurcation diagrams, the support of periodic or chaotic attractors, and dynamical stability.

In this work, we aim to overcome this limitation in implementing a specific DNO topology (case study) by using off-the-shelf digital components to verify and demonstrate experimentally the capability of DNOs to support complex dynamics. We qualitatively confirm both analysis and numerical simulations based on low-complexity models [1,3,5,14].

This work is organized as in the following. In Section 2, we introduce the proposed DNO case study within the theoretical framework of coupled oscillators. In Sections 3 and 4, we discuss the characterization of the dynamical behavior of the implemented circuit with experiments. The conclusion and references close the paper.

2. Case Study DNO: Design and Implementation

In many cases, as holds for the proposed case study, presented in the following section, DNOs can be viewed as networks of coupled oscillators. The dynamics of coupled oscillators has been studied for centuries, starting from the well-known synchronization of weakly coupled mechanical pendulums. This phenomenon is known as phase-locking and is generally present in dissipative systems with competing frequencies. Depending on both the system parameters and the coupling strength, different kinds of dynamics can be observed, ranging from periodic-locked and quasi-periodic (i.e., the ratio between the two oscillator frequencies is irrational) to chaotic. To have chaotic dynamics, a fundamental role is played by the nonlinear nature of both the oscillators and the coupling between them [16–20].

A special case of coupled oscillators is obtained when an autonomous dynamical system $\mathbf{x}$ is used to generate a driving signal, exciting a second dynamical system $\mathbf{y}$. In this situation, referring to a wide theoretical framework, the overall system can be described by the generic system of nonlinear differential equations

$$\begin{cases} \dot{\mathbf{x}} = \mathbf{f}(\mathbf{x}), \\ \dot{\mathbf{y}} = \mathbf{g}(\mathbf{x}, \mathbf{y}), \end{cases} \tag{1}$$

with $\mathbf{x} : \mathbb{R} \to \mathbb{R}^N, \mathbf{y} : \mathbb{R} \to \mathbb{R}^M$ being real-valued functions of time t, and $\mathbf{f}, \mathbf{g}$ being nonlinear smooth real-valued functions of $\mathbf{x}$ and $\mathbf{y}$, respectively. If $\dot{\mathbf{x}} = \mathbf{f}(\mathbf{x})$ and $\dot{\mathbf{y}} = \mathbf{g}(\mathbf{0}, \mathbf{y})$ define two periodic dynamical systems, we may call $\mathbf{y}$ in (1) the *forced oscillator*, with $\mathbf{x}$ being the *forcing periodic driver*, as shown in Figure 1.

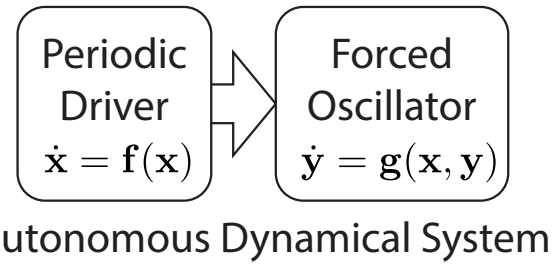

Figure 1. The architecture of the investigated nonlinear dynamical system.

In this work, by investigating a DNO in the analog domain, we investigate the implementation of the generic architecture shown in Figure 1 by properly combining commercial off-the-shelf components from the CD4000 series of CMOS logic chips. Standard 4000-series CMOS gates represent an established technology that has been available in the industry for decades. They are designed for power supply voltages ranging between 3 V and 18 V, used in a variety of electronic applications where low power consumption, have high noise immunity, and reliable operation over a wide range of operating conditions is required. Our proposal makes use of CD4049UB, CD4050B, CD4070B, and CD4077B by Texas Instruments functioning as inverting buffers, non-inverting buffers, XOR gates and XNOR gates, respectively. The circuit complexity of these digital gates has to be assessed by inspecting their schematics, as reported in Figure 2.

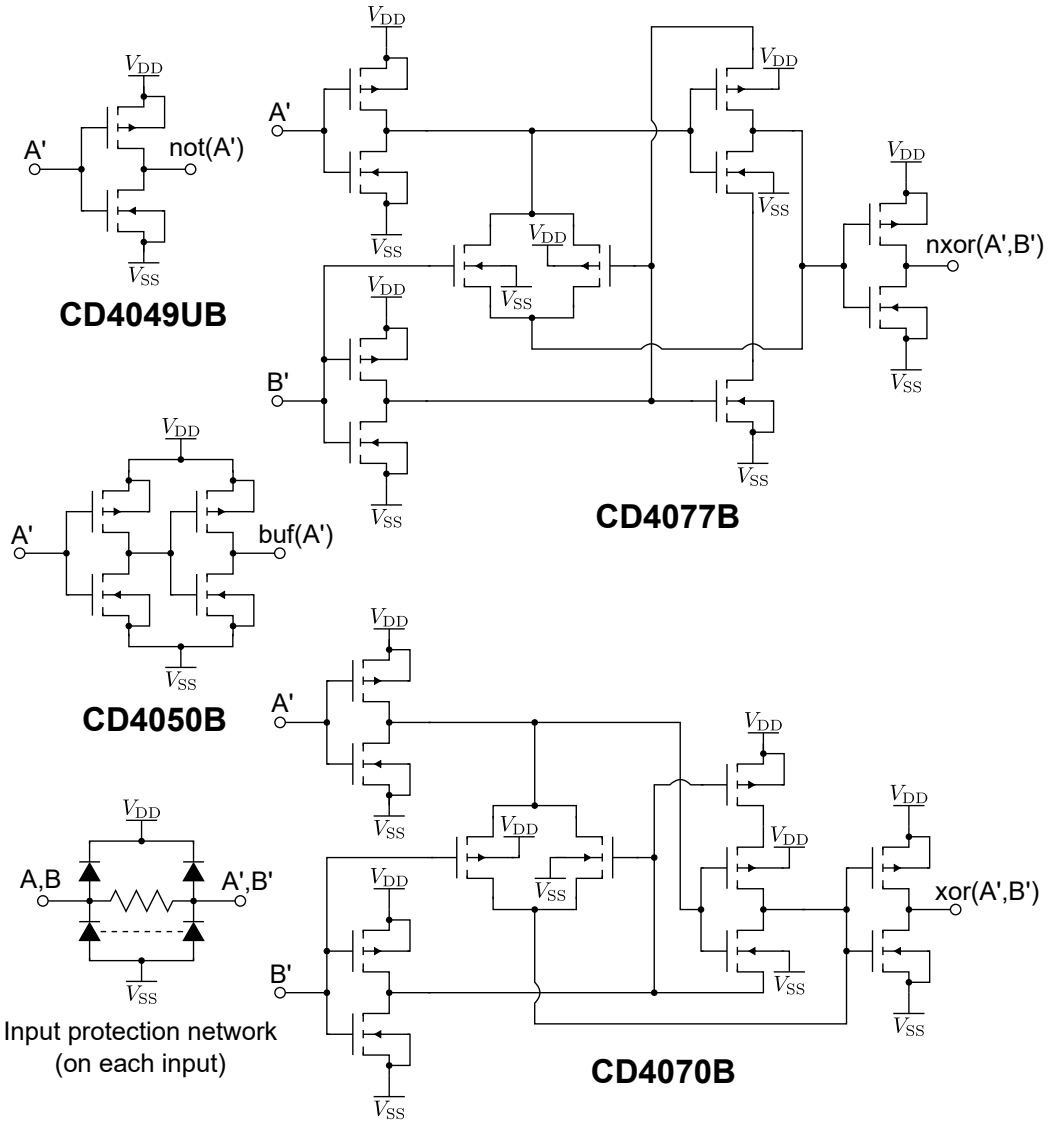

Figure 2. Schematic diagrams of the commercial off-the-shelf components used in this work from the CD4000 Series of CMOS logic chips by Texas Instruments. They function as inverting buffers (CD4049UB), non-inverting buffers (CD4050B), XOR gates (CD4070B), and XNOR gates (CD4077B).

As it can be appreciated from the figure, the inverting and non-inverting buffers are made of CMOS inverters, whereas in the XOR and NXOR gates, a network of CMOS inverters is completed by mixing tri-state and pass-transistor based glue logic. The complexity of the digital gates plays a relevant role in determining the mathematical dimension of the overall dynamical system. The distribution of parasitic capacitances, including a number of nonlinear capacitors related to the physical silicon MOSFETs are examined. From a theoretical point of view, the distributed charge in parasitic capacitors (that is related to node voltages by means of linear or non-linear relations) sets the state of the dynamical system ($\mathbf{x}$ and $\mathbf{y}$ in (1)) and evolves in the time-domain to determine different kinds of dynamics. Accordingly, it is clear from these considerations that dynamical systems associated to physical DNOs can have dimension in the order of tens or hundreds (i.e., $N + M \approx 10 \div 100$ in (1)), even considering low-complexity solutions.

The test bench designed to carry out the experiments presented in this work included a digital multimeter (Agilent 34410A), an oscilloscope (LeCroy WR44MXI), an arbitrary waveform generator (Agilent 33220A), and a programmable power supply (Agilent E3634A). All measurements were collected and analyzed using National Instruments LabVIEW and Mathworks MATLAB software tools.

As discussed in the following sections, the authors investigated the complete DNO architecture given in Figure 1. In detail, in Section 3, the implementation and analysis of the forced oscillator, which determines the chief characteristics of the DNO dynamical behavior, is first presented. In Section 4, the whole circuit, including the periodic driver, is discussed.

3. Forced Oscillator: Implementation and Analysis

The topology of the forced oscillator is shown in Figure 3, defining V_A, V_B and V_C the voltages at the nets to be A, B, C, respectively. The key elements of this circuit are the two ring oscillators obtained by combining an `xor` (`nxor`) gate and n delay elements (buffers) in a loop. The second input of the `xor` (`nxor`) gate is used to enable the oscillation, setting the operation of the `xor` (`nxor`) gate as an inverter if V_A is high (low). An xor gate is used to mix the state voltages of the two ring oscillators (voltages at the nodes B and C in Figure 3) and the driving excitation, providing the feedback mixing signal V_A.

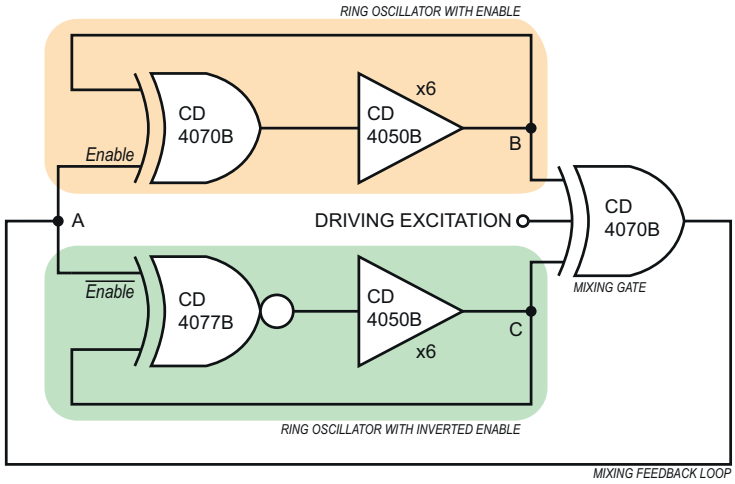

Figure 3. The low-complexity architecture of the forced oscillator.

Turned-Off Excitation: Dynamical Behavior

The operation of the two ring oscillators is shown in Figure 4, assuming the mixing feedback loop open and the enabling voltage V_A to be externally driven by a square wave obtained from a signal generator. The oscillation of the sub-circuits is assured when the number of CMOS stages involved in the loop is greater than two [14]. Accordingly, the minimum number of off-the-shelf components to trigger oscillations depends on their CMOS internal architecture. To slow down the dynamics in this work, we used six CD4050B buffers. The choice allowed for the empirical rough tuning of the oscillation frequencies of the two loops. The loops are slightly asymmetric due to the differences in the internal architecture of the `xor` and `nxor` gates (Figure 2). According to the measurement results, the oscillation frequency of the two ring oscillators resulted in $f_{\mathrm{RO}} \approx 3.6$ MHz at room temperature (22 °C) for a power supply voltage of $V_{dd} = 6$ V and $V_{ss} = 0$ V. The oscillation frequencies of the two circuits resulted in slightly different (in the order of tens of kHz) due to several aspects including differences in the internal architectures of the CD4077B and CD4070B gates, process variability, and residual parasitic unbalance in the implemented connectivity among elements. On average, considering the number of stages (i.e., seven in each loop), the corresponding theoretical mean propagation delay resulted in $t_p \approx 10^6/(2 \times 7 \times 3.6) \approx 19.8$ ns for each gate [21,22].

It is worth recalling that in this kind of oscillator, the oscillation frequency weakly depends on the temperature and strongly depends on the power supply voltage, depending on both the technology and the hardware implementation [23–25]. In more detail, it is well known from the literature that the propagation delay of CMOS logic gates increases with temperature. This affects transistor threshold voltages, charge carrier mobilities, and

saturation velocities, among other features [23–25]. As a result, the combined effect of a temperature increase on a CMOS digital gate operated at its nominal power supply voltage is a reduction of its output current and causes circuit speed degradation.

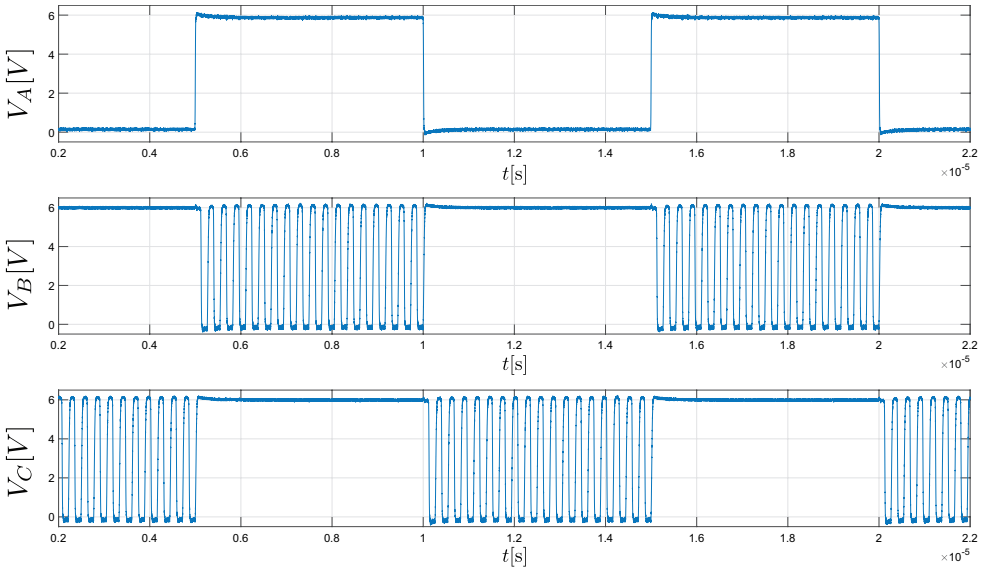

Figure 4. The operation of the two ring oscillators in Figure 3, assuming an open mixing feedback loop and that the enabling voltage V_A is externally driven by a waveform generator as a square wave.

For the sake of our study, we investigated the dependency of the oscillation frequency with the power supply voltage at a constant room temperature (22 °C), viewing the circuits as Voltage-Controlled Oscillators (VCOs).

From this point of view, since propagation delays in CMOS logic gates decrease with increments of $V_{dd} - V_{ss}$ [23–25], the oscillation frequency increases with the power supply voltage, as expected from ring oscillator modeling [21,22], as shown in Figure 5. Referring to the experimental results reported in this figure, the theoretical mean propagation delay per gate varies between $t_p \approx 8.1$ ns and 79.3 ns for supply voltages $V_{dd} - V_{ss} = 3$ V and 18 V, respectively [21,22].

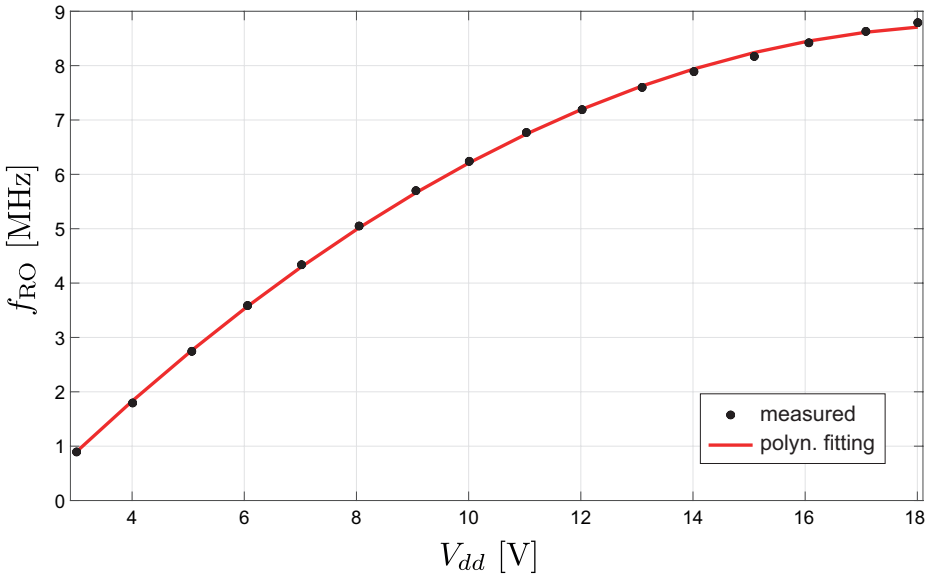

Figure 5. The measured oscillation frequency of the ring oscillators in Figure 3, as a function of V_{dd}, and a corresponding polynomial fitting $f_{\mathrm{RO}}(V_{dd}) \approx \alpha V_{dd}^2 + \beta V_{dd} + \gamma$, where $\alpha = -0.0298$ Hz/V^2, $\beta = 1.147$ Hz/V, $\gamma = -2.283$ Hz.

Furthermore, it is worth noting that a change in the power supply voltage affects both the static and dynamical properties of the circuit, as shown in Figure 6. We stress an important consequence of this fact: differently from digital circuits implementing boolean functions independent from the power supply voltage, in DNOs, the power supply voltage plays a relevant role in determining the dynamical behavior of the nonlinear circuit (this aspect is made more clear in the next section).

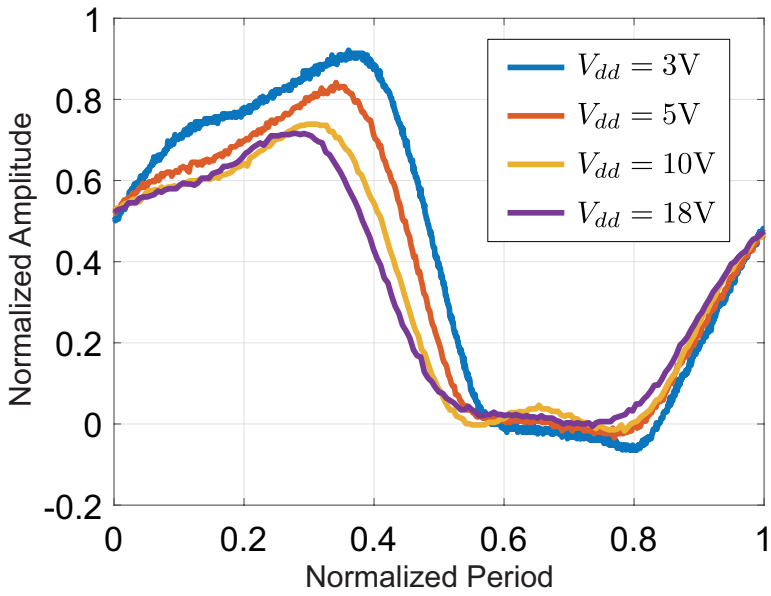

Figure 6. The dynamical behavior of the ring oscillator for different supply voltages.

As expected from low-complexity numerical modeling [1], when the driver excitation is turned off, the implemented dynamical system $\dot{\mathbf{y}} = \mathbf{g}(\mathbf{0}, \mathbf{y})$ in Figure 3 resulted in a periodic oscillator with a strongly attractive limit cycle, as shown in Figure 7 for $V_{dd} = 6$ V. The support of the limit cycle in the normalized phase space $(V_A/V_{dd}, V_B/V_{dd}, V_C/V_{dd})$ resulted in weakly dependent on V_{dd}, confirming the structural periodic stability of the system dynamical behavior when the excitation is turned off.

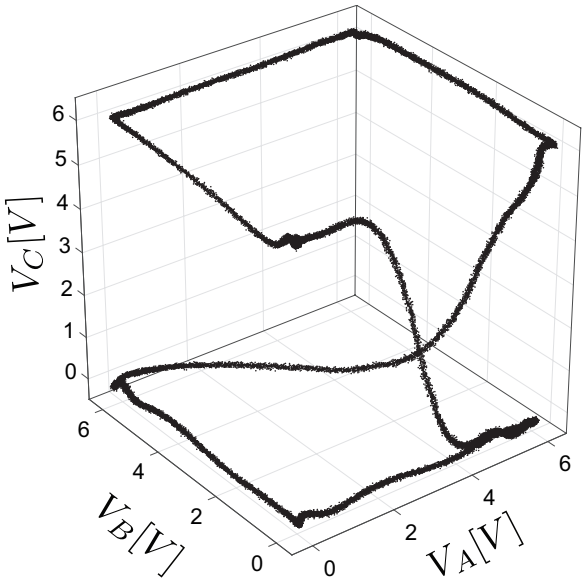

Figure 7. The strongly attractive limit cycle of the oscillator in Figure 3 when the driving excitation is turned off ($V_{dd} = 6$ V, 20 cycles reported). The periodic trajectory had a measured frequency $f_0 \approx 1.87$ MHz).

We investigated the dynamical behavior of the forced oscillator when a periodic excitation is applied to its input: namely, a square wave with levels 0 V and V_{dd} at different frequencies (e.g., a clock signal). The experiments were conducted considering different supply voltage levels for excitation frequencies ranging between 500 kHz and 5 MHz.

As expected from numerical modeling of DNOs [1], experiments confirmed that by smoothly changing the excitation frequency, the system exhibits multiple attracting sets, triggers different dynamics, and partitions the phase state in disjoint basins of attraction dependent on both the supply voltage and the excitation frequency. Typical measurement results are summarized in the bifurcation diagram shown in sub-plot a in Figure 8. Excitation frequencies range between 1 MHz and 2 MHz and are obtained as described in the following text.

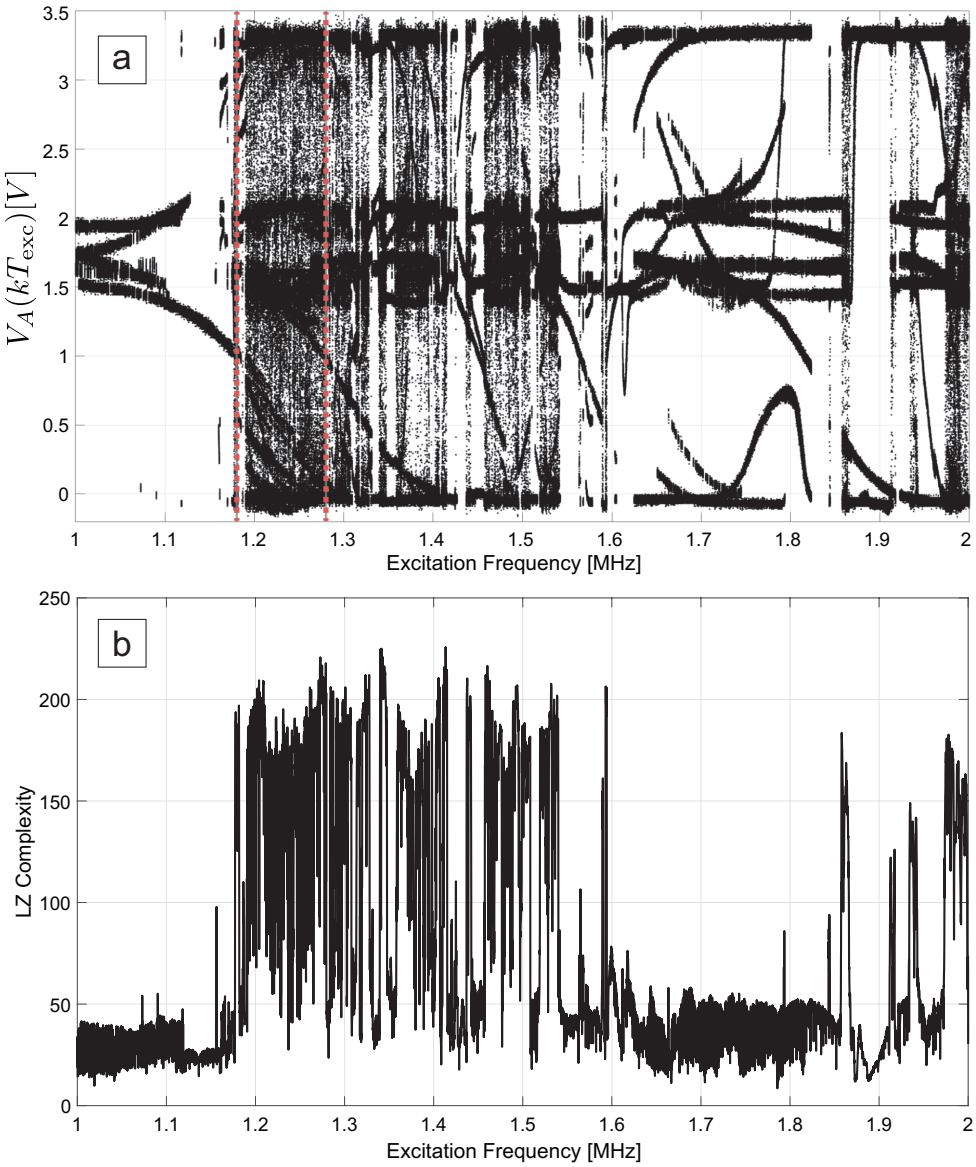

Figure 8. Sub-plot (**a**): Bifurcation diagram for the dynamical system in Figure 3 reporting the measured voltages (2) for excitation frequencies ranging between 1 MHz and 2 MHz (100 Hz sweep step) and a supply voltage of 3.3 V. The two vertical marker lines at $f_{\rm exc} = 1.1975$ MHz and $f_{\rm exc} = 1.1982$ MHz delimit the sub-domain magnified in Figure 9. Sub-plot (**b**): The average Lempel–Ziv complexity computed for the symbolic sequences (3).

For each tested frequency (100 Hz sweep step), the excitation signal and the voltages at the nodes A, B, and C in Figure 3 have been acquired with a four-channel oscilloscope

recording 100 excitation cycles. To investigate the synchronization between the forced oscillator and the periodic driver, we computed the set of $k = 100$ voltages from the signal acquisitions

$$\left\{ V_A\left(t = \frac{k}{f_{\text{exc}}}\right), k \in \mathbf{N} \right\} \tag{2}$$

for each tested excitation frequency f_{exc}, assuming $t = 0$ as the first acquisition time at which the excitation signal crosses the reference threshold level $V_{dd}/2$.

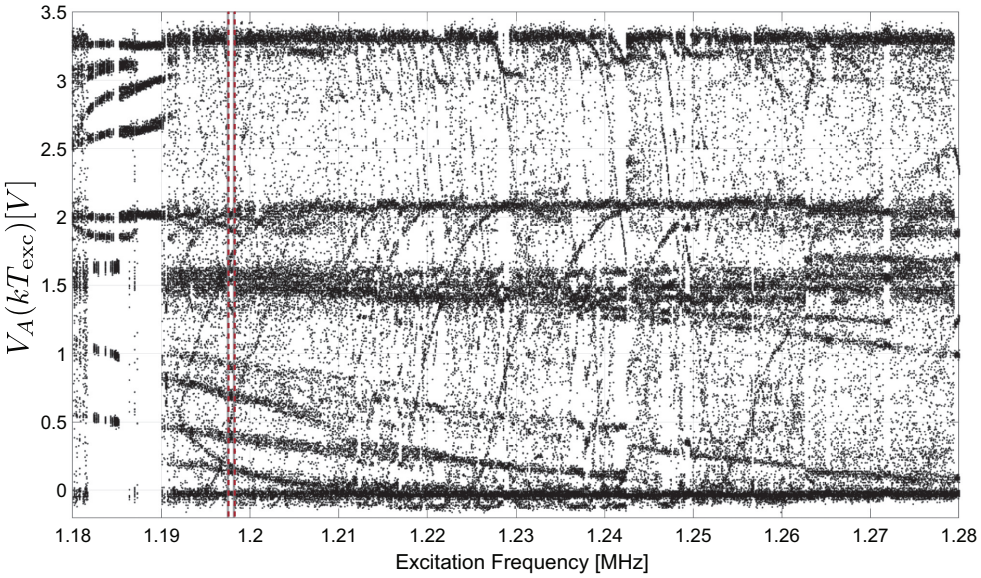

Figure 9. Magnification of the bifurcation diagram shown in Figure 8. The red vertical markers highlight one of the several small detected periodic windows in the investigated frequency range.

Both chaotic and periodic behaviors were confirmed independently from the time phase (i.e., the reference threshold level setting the acquisition time $t = 0$) and obtained similar results for different supply voltages (3 V $\leq V_{dd} \leq$ 18 V) and excitation frequencies (500 kHz–5 MHz). In detail, to assess the complexity of the dynamics, for each test frequency f_{exc} in the bifurcation diagram range, we processed the sequence of voltages (2) to build symbolic sequences $\mathcal{S} = \{s_0, s_1, \ldots, s_k\}$, defined as

$$s_k = \left\lfloor \frac{1 + V_A(kT_{\text{exc}})}{V_{dd} + 2} \cdot 8 \right\rfloor, \qquad s_k \in \{0, 1, \ldots, 7\}, \tag{3}$$

i.e., the levels $V_A(kT_{\text{exc}})$ have been properly shifted, scaled and three-bit quantized (eight levels). Once the symbolic sequence $\mathcal{S}$ was obtained, we evaluated its Lempel–Ziv complexity [26]. The process was repeated 100 times for each tested excitation frequency, collecting symbolic sequences of 1000 symbols ($k = 0, \ldots, 999$). The means of the measured Lempel–Ziv complexity have been reported in sub-plot b in Figure 8. The two vertical marker lines at $f_{\text{exc}} = 1.1975$ MHz and $f_{\text{exc}} = 1.1982$ MHz delimit the sub-domain magnified in Figure 9.

Further investigations were carried out analyzing the signal autocorrelation function, inspecting the acquisition trajectories in four-dimensions (excitation and A, B, and C node voltages) and Fourier analyses. As examples, we report two different periodic dynamical behavior and a chaotic dynamical behavior detected at excitation frequencies of 1,351,400 Hz, 1,390,100 Hz, and 1,377,600 Hz, respectively, for a nominal power supply of 6 V in Figure 10. On the left side of this figure, the evolution for a time interval equal to 100 excitation periods of the acquired signals is shown as trajectories in the voltage phase space (V_A, V_B, V_C). On the right side, the autocorrelation function $R_{xx}(\frac{t}{T_{\text{exc}}})$ for the voltage signal V_A is reported.

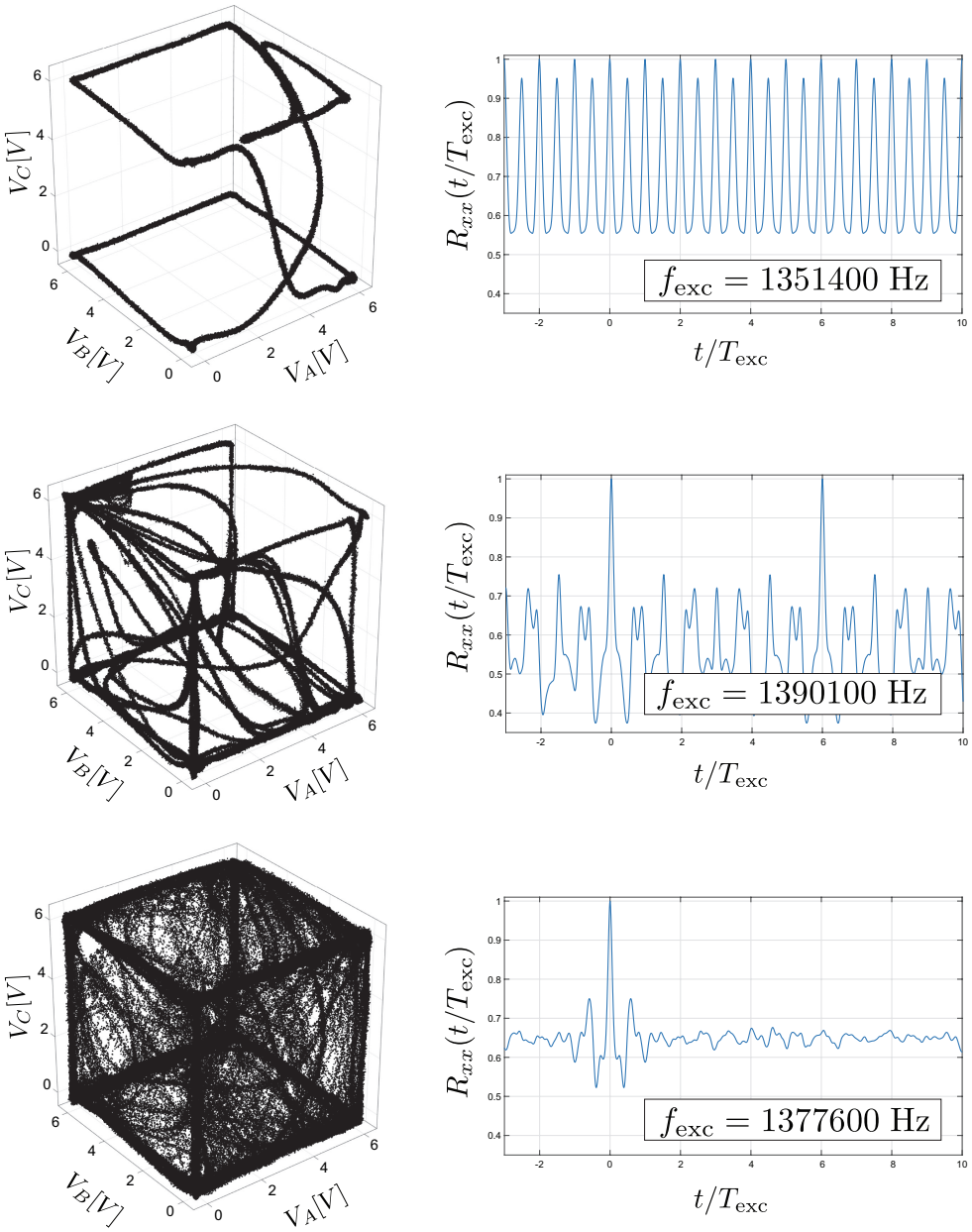

Figure 10. Two periodic dynamics (with periods $T_{\rm exc}$ and $6T_{\rm exc}$) and a chaotic dynamics detected at nominal excitation frequencies 1,351,400 Hz, 1,390,100 Hz, and 1,377,600 Hz, respectively, for a power supply of 6 V. The autocorrelation function refers to the voltage signal V_A.

As shown by the autocorrelation function, in the first periodic case ($f_{\rm exc} = 1{,}351{,}400$ Hz), the limit cycle of the forced oscillator has period $T_{\rm exc}$, whereas in the second periodic case ($f_{\rm exc} = 1{,}390{,}100$ Hz), it is equal to $6T_{\rm exc}$, exhibiting a quite complex, stable support. In the last case ($f_{\rm exc} = 1{,}377{,}600$ Hz), the dynamics is fully chaotic. Several chaotic windows can be spotted in the bifurcation diagrams shown in Figures 8 and 9 in an interval associated to complex dynamics (high entropy). At closer inspection, chaotic regions are interleaved with (more or less complex) periodic windows as expected from the simulation of low-complexity DNOs dynamical models [1].

4. Overall DNO Circuit Analysis

The complete architecture shown in Figure 1 has been investigated driving the forced oscillator with an autonomous ring oscillator, as shown in Figure 11.

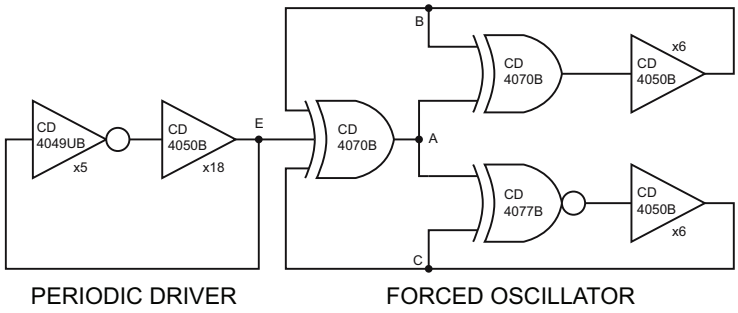

Figure 11. The implemented architecture of the complete DNO.

To slow down and roughly tune the oscillation frequency around the previously investigated excitation frequency ranges, the periodic driver was implemented using 5 inverting gates (CD4049UB) and 18 buffers (CD4050B). Considering the schematics shown in Figure 2, the implemented solution counts 41 CMOS inverters. As it happens for the oscillating sub-circuits in Figure 3, the oscillation frequency of the periodic driver depends on the power supply voltage, following a trend similar to the one shown in Figure 5. In this case, the oscillation frequency ranged between 320 kHz ($V_{dd} = 3.3$ V) and 2.785 MHz ($V_{dd} = 18$ V).

Adopting the investigation approach discussed in Section 3, we derived a bifurcation diagram referring to the power supply voltage as the bifurcation parameter, as shown in Figure 12. In more detail, for each tested power supply voltage (2 mV sweep step), the excitation signal and the voltages at nodes A, B, C, and E in Figure 11 have been acquired with a four-channel oscilloscope, recording 100 excitation cycles. To investigate the synchronization between the forced oscillator and the periodic driver, we computed a set of $k = 100$ voltages from the signal acquisition for each tested power supply voltage V_{dd}. Since V_{dd} also affects the amplitude of the dynamics, the acquired voltages have been properly normalized, i.e.,

$$\left\{ x_A(k) = \frac{V_A(t_k)}{V_{dd}}, k \in \mathbf{N} \right\}, \tag{4}$$

where $\{t_k\}$ is the sequence of times at which the periodic excitation voltage V_E crosses the threshold $V_{dd}/2$ with a rising edge.

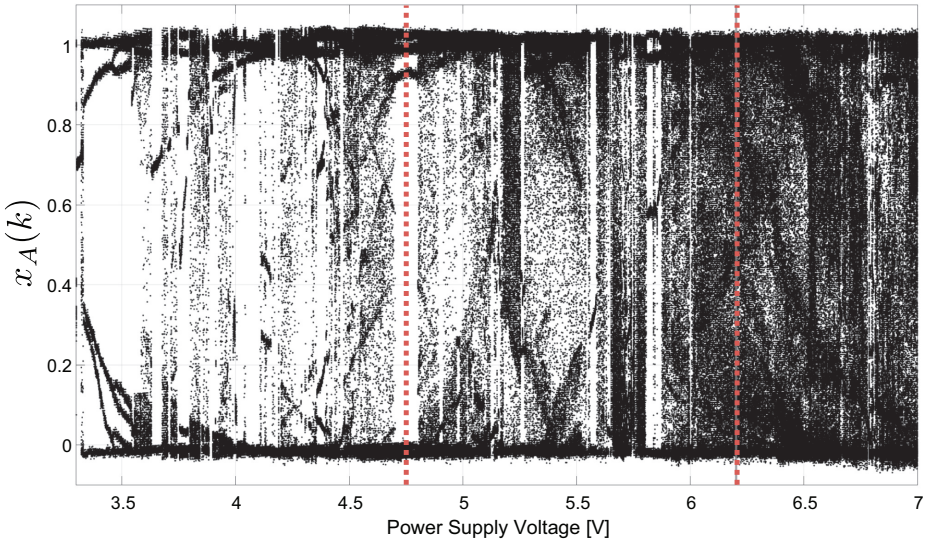

Figure 12. Bifurcation diagram for the dynamical system in Figure 11 reporting the measured normalized voltages (4) for power supply voltage ranging between 3.3 V and 7 V (2 mV sweep step). The vertical marker lines at $V_{dd} = 4.7$ V and $V_{dd} = 6.2$ V identify the power supply voltages set for the experiments presented in Figure 13 and Section 4.1.

The bifurcation diagram highlights the presence of chaotic and periodic windows as a function of the applied supply voltage. For example, in Figure 13, it is possible to observe how a voltage $V_{dd} = 4.7$ V, corresponding to an excitation frequency $f_{\text{exc}} \approx 691$ kHz, reveals periodic dynamics with period equal to $6T_{\text{exc}}$, while a voltage $V_{dd} = 6.2$ V, corresponding to an excitation frequency $f_{\text{exc}} \approx 1038$ kHz, leads to chaotic dynamics.

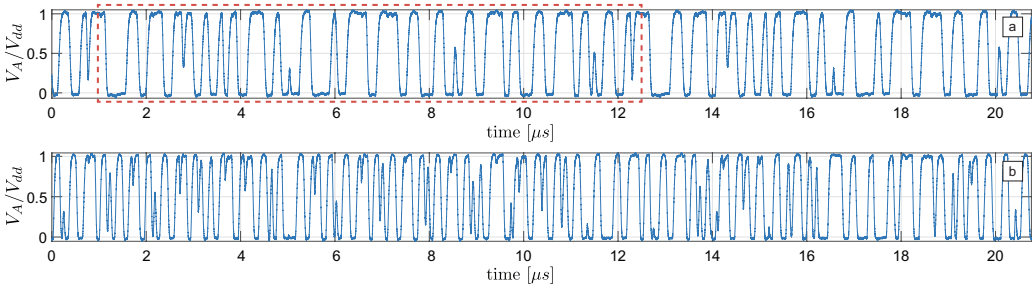

Figure 13. Two acquired V_A signals for different supply voltages. Sub-plot (**a**): $V_{dd} = 4.7$ V, corresponding to an excitation frequency $f_{\text{exc}} \approx 691$ kHz, revealing periodic dynamics with period equal to $6T_{\text{exc}}$ (highlighted). Sub-plot (**b**): $V_{dd} = 6.2$ V, corresponding to an excitation frequency $f_{\text{exc}} \approx 1038$ kHz, revealing chaotic dynamics.

The corresponding Lempel–Ziv complexity is shown in Figure 14. Interestingly, the entropy of the dynamical system resulted higher than in the previous case (i.e., when the forced oscillator was driven by a signal generator). This is mainly because the periodic driver is itself a well known source of information, considering the jitter introduced by electronic noise, boosting the complexity of the dynamics. This is beneficial for most applications that focus on the design of entropy sources for cryptographic applications.

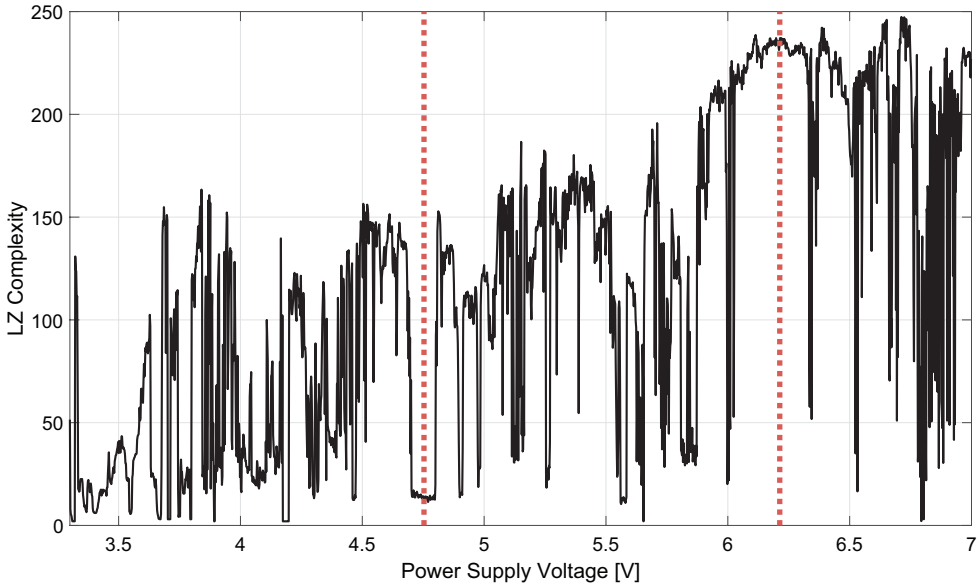

Figure 14. The average Lempel–Ziv complexity computed for the symbolic sequences (3), for the dynamical system in Figure 11, and a power supply voltage ranging between 3.3 V and 7 V (2 mV sweep step). The vertical marker lines at $V_{dd} = 4.7$ V and $V_{dd} = 6.2$ V identify the power supply voltages set for the experiments presented in Figure 13 and Section 4.1.

4.1. Randomness and Statistical Tests

As a final confirmation to assess the capability of the investigated DNO to generate complex signals, we used the circuit shown in Figure 11 as an entropy source to design a true random number generator passing the NIST 800.22 standard tests for cryptographic randomness [27]. Accordingly, the power supply voltage has been set to 6.2 V; that is, a

value that is among the power supply voltages corresponding to chaotic dynamics in the bifurcation diagram and the highest Lempel–Ziv complexity in Figures 12 and 14. At this value of V_{dd}, the oscillation of the driver results in $\approx$ 1.038 MHz. In this setup, the signal V_A has been uniformly sampled and one-bit quantized according to a sampling frequency of 100 kHz. It is worth noting that such a low throughput is coherent with the dynamics of the circuit, which, in this demonstrator, has been intentionally reduced 100 $\div$ 1000 times with respect to what is typically achieved in integrated circuits [1].

Consistent with NIST recommendations and to mitigate the residual statistical defects of the random binary sequences and pass the tests, the random stream has been post-processed with a low-complexity stream cipher, performing the bit-by-bit XORing of the collected raw bits with an eight-bit pseudo-random generator (a Fibonacci LFSR based on the primitive polynomial $x^8 + x^4 + x^3 + x^2 + 1$). In Table 1, the obtained results for the NIST tests are reported on the basis of 100 binary sequences of 10^6 collected bits.

Table 1. NIST 800.22 rev.1a Statistical Tests Results.

Test Name	*p*-Value	Proportion	Result
Frequency	0.897763	1.00	*pass*
BlockFrequency	0.719747	0.97	*pass*
CumulativeSums [a]	0.637119	0.99	*pass*
Runs	0.514124	0.96	*pass*
LongestRun	0.455937	0.99	*pass*
Rank	0.042808	1.00	*pass*
FFT	0.657933	0.97	*pass*
NonOverlappingTemplate [a]	0.739918	0.96	*pass*
OverlappingTemplate	0.851383	0.99	*pass*
Universal	0.595549	0.97	*pass*
ApproximateEntropy	0.030806	0.99	*pass*
RandomExcursions [a]	0.051391	0.97	*pass*
RandomExcursionsVariant [a]	0.116519	0.98	*pass*
Serial [a]	0.275709	0.99	*pass*
LinearComplexity	0.102526	0.99	*pass*

[a] Worst case reported for tests with multiple outcomes.

5. Conclusions

A specific topology of Digital Nonlinear Oscillators (DNOs) has been implemented by using commercial off-the-shelf digital components to experimentally verify and demonstrate the capability of these circuits to support complex dynamics, independently from their implementation technology. The implemented test bench made it possible to monitor the electrical dynamics of the DNO at an analog level, allowing for investigation of numerous aspects related to the complex dynamics of the nonlinear system, such as the analysis of bifurcation diagrams, the support of periodic or chaotic attractors, and dynamical stability. The autonomous circuit has been investigated as a source of entropy, adopting different figures of merit, including the Lempel–Ziv complexity, to evaluate the dynamics measured under different operating conditions. Furthermore, the entropy source has been also assessed for the possible design of low-complexity TRNGs and is capable of passing the NIST 800.22 tests, confirming the applicability of this class of circuits in the context of lightweight cryptography.

The obtained results demonstrate that DNOs can support complex dynamics and exhibit periodic and chaotic dynamical behaviors, depending on different design aspects such as the power supply voltage. At the same time, focusing on the cryptographic reliability of this kind of solutions, experimental results pose the problem of the control of the system entropy, taking into account its manifested sensitivity with respect to different implementation aspects under the weak control of the designer. The authors are currently investigating the possible use of feedback strategies to gain control of the circuit entropy.

Author Contributions: Conceptualization, T.A. and R.M.; methodology, T.A., R.M. and F.S.; software, R.M. and F.S.; validation, R.M. and F.S.; formal analysis, T.A. and R.M.; investigation, T.A., R.M. and F.S.; resources, T.A., A.F. and V.V.; data curation, R.M.; writing—original draft preparation, T.A., R.M. and F.S.; writing—review and editing, T.A., A.F. and V.V.; visualization, T.A. and R.M.; supervision, T.A., A.F. and V.V.; project administration, T.A., A.F. and V.V.; funding acquisition, T.A., A.F. and V.V. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Data Availability Statement: Data is available upon request to the authors.

Conflicts of Interest: The authors declare no conflict of interest.

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