Chua's Circuit With Tunable Nonlinearity Based on a Nonvolatile Memristor: Design and Realization

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***Abstract*— Nonvolatile memristive devices display nonlinear characteristics suitable for implementing circuits exhibiting oscillations or more complex dynamic behaviors, including chaos. However, the results presented in related works are mostly limited to simulations and employing ideal memristor models whose resistance is governed by a charge-flux relation that is not connected to real devices, thus hindering the realization of such nonlinear oscillators. In this work, we present the framework for the physical implementation of a tunable memristor Chua's circuit, which is based on a nonvolatile memristive device that provides the nonlinear conductance required by the circuit and the possibility to tune it for the purpose of selecting among different oscillation patterns. We first establish design guidelines to guarantee complex oscillations in the tunable memristor Chua's circuit. Further, we physically implement the circuit after characterizing and modeling the tunable current-voltage characteristic of a real device. Our circuit successfully generates different oscillation patterns just by programming the nonvolatile memristive device to different states. The devised design guidelines and device modeling were used to extend the experimental work and draw further requirements for device properties for a successful circuit implementation.**

***Index Terms*— Memristor, memristor circuits, RRAM, chaos, nonlinear circuits, oscillators.**

I. Introduction

NONLINEAR oscillators are systems with rich dynamics that can be employed as a primitive in several applications. The complex interactions in networks of interconnected oscillators have been exploited to address problems with no efficient solutions on von-Neumann machines, such as pattern recognition [1] and solving combinatorial problems [2]. Under certain circumstances, some nonlinear oscillators can even exhibit chaos—aperiodic oscillation patterns that are unpredictable due to their extreme sensitivity to the initial conditions— [3]. Although apparently undesirable, chaos has been proven beneficial in applications related to secure communications [4], sensor conditioning [5] and hardware implementation of optimization problems [6].

The integration of nonlinear oscillator circuits has been typically hindered by the lack of technological realizations providing low-power and high-scalable solutions. However, this scenario changed with the research advancements in the pursuit of novel material properties to surpass the physical limits present in CMOS-based machines. In this context, different emerging circuit elements to be used as part of the implementation of nonlinear oscillators have been proposed [7]. Among them, memristive devices are one of the most promising. Memristive devices are two-terminal electrical components that switch their resistance state by the application of a stimulus. Although memristive devices are mainly praised as memory elements due to their nonvolatile properties, they can also exhibit nonlinear and dynamic attributes, such as threshold switching, volatile switching, or negative differential resistance [8]. All these properties are of interest for implementing nonlinear oscillators. The dynamic properties of some memristive devices are usually more attractive. For instance, the resistive switching dynamics of nonvolatile memristive devices are used in relaxation oscillators [9] or to enhance the dynamic behavior in chaotic circuits [10], [11], [12]. Furthermore, the metal-insulator transition in Mott memristors paved the way towards extremely compact oscillators exhibiting self-sustained periodic oscillations [13], [14], [15], and even chaotic patterns [16]. Instead, nonvolatility has rarely been exploited in oscillators; the only example found consists in employing the memristive device as a programmable resistor in conventional relaxation oscillators [17].

We propose a physical implementation of a nonlinear oscillator with a nonvolatile memristive device, in which the device improves the circuit scalability and provides additional features. For this purpose, we chose to implement a memristive version of Chua's nonlinear oscillator circuit. Known as the simplest autonomous chaotic oscillator, Chua's circuit requires a nonlinear resistor to exhibit chaos, and additionally, a mechanism to modify one or more of Chua's circuit elements to generate different dynamic behaviors [18], [19]. A single nonvolatile memristive device can address both requirements by using it as a tunable nonlinear resistor. But the physical realization of such a memristive version comes with

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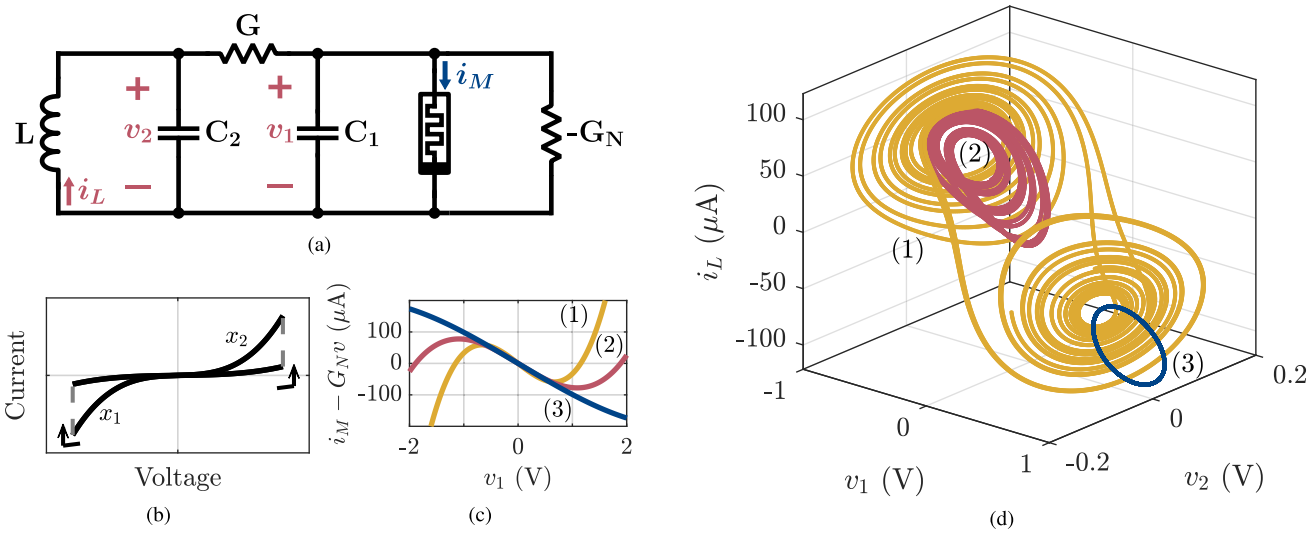

Fig. 1. Tunable memristor Chua's circuit. (a) Circuit scheme. (b) Typical experimental i-v curve of a bipolar memristor. (c) Examples of possible currents for the nonlinear part implementable with a memristor in parallel with a negative conductance $-G_N$, where (1) to (3) indicate low to high contribution of nonlinear terms in the memristor current. (d) Circuit trajectories generated with the example currents from (c) and fixed Chua's circuit parameters $G = 0.1$ mS, $C_1 = 1$ nF, $C_2 = 10$ nF and $L = 70$ mH.

some challenges. First, the characterization of a nonvolatile memristive device as a tunable nonlinear resistor has not been extensively studied, or at the very least, it has not been used in applications since it is typically unwanted [20]. Second, although Chua's circuit has been thoroughly analyzed, the same does not hold true when it is implemented in connection with a tunable nonlinear resistor.

To our best knowledge, the idea of substituting the conventional nonlinear resistor in Chua's circuit with a memristive device has never been physically implemented with a real memristive device. While the circuit concept already exists, most of the work has been limited to simulations by using memristive models that are not representative of real devices [21], [22]. Therefore, the opportunity to establish the foundations for the implementation of Chua's circuit with real memristive devices is yet to come. It is worth mentioning that while [11], [12] implement different modified versions of Chua's circuit by introducing real memristive devices, both of them do not replace the nonlinearity required for generating chaos. Therefore, the memristive device neither plays an exclusive role in chaos generation nor adds control to the system's dynamic response.

In this work, we build upon the preliminary results reported in [23] to present a comprehensive framework for a hardware realization of a tunable memristor Chua's circuit, i.e., a Chua's circuit with a tunable nonlinear element based on a nonvolatile memristive device. We model the memristive device as a tunable nonlinear resistor. The model provides a direct link between the device resistive state, the tunable memristor Chua's circuit design and its experimental verification. Moreover, it also allows us to determine which are the opportunities and limitations of the circuit regarding device properties and design choices, assisted by numerical simulations.

The rest of the paper is organized as follows. Section II introduces the tunable memristor Chua's circuit and basic design guidelines to ensure correct operation considering a tunable nonvolatile memristive device. Section III reports the device electrical characteristics and modeling as a tunable nonlinear resistor, the circuit design and experimental verification. Section IV discusses the most critical device properties for implementing the tunable memristor Chua's circuit, assisted by numerical simulations. Conclusions are drawn in Section V. This framework can be adapted to other circuits that require similar nonlinear elements, like the Bonhoeffer-van der Pol [24] or Murali-Lakshmaann-Chua [25] oscillators.

II. Tunable Memristor Chua's Circuit

A. Circuit Description

The scheme of the tunable memristor Chua's circuit is depicted in Fig. 1(a). The inductor L, capacitors C_1 and C_2, and conductance G form the linear part of the circuit, while the rightmost side corresponds to the nonlinear part. We propose a tunable nonlinear part based on a threshold-switching nonvolatile memristive device working as a programmable nonlinear resistor. For the sake of brevity, the term memristor will be used from now on instead of nonvolatile memristive device. A typical memristor exhibits a current that is nonlinear with respect to voltage and associated with the device resistance state. The resistive state is defined by memristor internal state variables, which are different according to the underlying memristor switching mechanism. In our work, we group any relevant state variable into the internal state x. For a threshold-switching memristor, when the applied voltage exceeds certain levels, the internal state x can be tuned, thus changing the current flowing through the memristor. Fig. 1(b) exemplifies the typical i-v characteristic of a memristor when programmed at two different states. The memristor behavior can be mathematically described using the concept of the extended memristor as

$$\begin{aligned} i &= i(v, x) \\ \frac{dx}{dt} &= h(v, x) \end{aligned} \tag{1}$$

The memristor behaves as a nonlinear resistor when it is operated within its non-switching region, i.e., at a voltage domain at which $h(v, x) = 0$. From now on, we formalize the memristor current within the non-switching region as $i_M(v, x)$ and its differential conductance as $G_M(v, x) = di_M/dv$, where both quantities are dependent on the memristor internal state. It is worth noticing that G_M is different from the definition of memductance i_M/v.

Chua's circuit requires a nonlinear part with an active conductance to produce oscillations and chaos. As it may be noticed in Fig. 1(b), memristors do not exhibit active conductance in their quasi-static characteristics. We overcome this issue by splitting the tunable nonlinear part features into the parallel of two devices: the memristor and a negative linear conductance $-G_N$. As a result, the memristor provides a nonlinear conductance with robust tunability features, while $-G_N$ shifts the memristor current that results in a nonlinear part with an overall active conductance. For the nonlinear part to effectively exhibit active conductance, G_N must be higher than the memristor differential conductance G_M at low voltages. Fig. 1(c) illustrates examples of the overall nonlinear part i-v characteristics by employing a fixed G_N value and an arbitrary i_M tuned at different x.

Chua's circuit response is defined by the state variables v_1, v_2, and i_L. The time-ordered collection of states (v_1, v_2, i_L) is referred to as the circuit trajectory. Depending on the circuit impedance values from the linear part of the circuit and parameters from the nonlinear part, the circuit can show different periodic or chaotic trajectories. Fig. 1(d) shows the trajectories generated in a circuit simulation using the nonlinear functions from Fig. 1(c) in a Chua's circuit with fixed linear impedances. We refer to trajectories 1, 2, and 3 as symmetric aperiodic, asymmetric aperiodic, and asymmetric periodic, respectively; trajectories 1 and 2 are also known in the literature as double-scroll and single-scroll. It may be noted that the trajectories orbit around one or two points, depending on whether the trajectory is asymmetric or not with respect to the origin $v_1 = v_2 = i_L = 0$.

It is important to distinguish that the tunable memristor Chua's circuit has two modes of operation: the programming mode and the oscillation mode. In the programming mode, the circuit is not oscillating and the memristor state x is tuned. During oscillation mode, the circuit is powered up and generates an oscillating pattern. In this mode, the characteristics of the nonlinear part are static ($h(v, x) = 0$), and thus x is not changed. The memristor in Fig. 1(a) directly faces v_1 as generated by the tunable memristor Chua's circuit, such as the ones shown in Fig. 1(b). Therefore, during the programming mode, high voltage levels are applied for tuning x, whereas v_1 must be contained between the memristor non-switching region to avoid modifying x during the oscillation mode.

B. Circuit Design Considerations

Chua's circuit is able to generate multiple oscillation patterns, such as the ones previously shown in Fig. 1(d). However, these patterns may only be possible in a small range of impedance values for the circuit linear part. Furthermore, they must be adapted to the spectrum of available i-v characteristics of the nonlinear part, which can be tuned through the memristor. This is particularly challenging in tunable memristor Chua's circuit, since the nonlinear part i-v characteristics are tunable, and the voltage applied across the memristor must be limited during the circuit oscillation mode. Therefore, all these constraints are next addressed with design guidelines, establishing minimum conditions for the memristor differential conductance G_M, and some critical impedance values in the circuit.

We are interested in the oscillation patterns generated due to the existence of a Hopf bifurcation, i.e., the birth of a periodic oscillation from equilibrium, that evolves to chaos through an infinite sequence of period-doubling bifurcations [18]. The trajectories depicted in Fig. 1(d) represent some examples of the oscillation patterns found in these aforementioned situations. The conditions required for exhibiting such trajectories have been widely reported in previous works by studying the stability of Chua's circuit dynamic system [26], [27], [28]. Next, we extend these results to the tunable memristor Chua's circuit, focusing on the tunable nonlinear part.

Two mathematical objects are used for the analysis: the dynamical system that describes the tunable memristor Chua's circuit from Fig. 1(a) as

$$\begin{aligned}\frac{dv_1}{dt} &= \frac{1}{C_1}\left(G(v_2 - v_1) - i_M(v_1, x) + G_N v_1\right)\\ \frac{dv_2}{dt} &= \frac{1}{C_2}\left(G(v_1 - v_2) + i_L\right)\\ \frac{di_L}{dt} &= -\frac{1}{L}v_2\end{aligned} \tag{2}$$

and its Jacobian matrix J

$$J = \begin{bmatrix} -\frac{G+G_M(v_1,x)-G_N}{C_1} & \frac{G}{C_1} & 0 \\ \frac{G}{C_2} & -\frac{G}{C_2} & \frac{1}{C_2} \\ 0 & -\frac{1}{L} & 0 \end{bmatrix} \tag{3}$$

Classical Chua's circuit works as a nonlinear oscillator when it has three equilibrium points (EP). EPs are constant solutions of the dynamic system in (2), i.e. satisfying $dv_1/dt = dv_2/dt = di_L/dt = 0$. Assuming odd symmetric memristor current i_M like the examples depicted in Fig. 1(b), the EPs for the tunable memristor Chua's circuit are

$$\begin{aligned}P_0 &= \{v_1 = v_2 = i_L = 0\}\\ P_+ &= \{v_1 = V_P, v_2 = 0, i_L = -GV_P\}\\ P_- &= \{v_1 = -V_P, v_2 = 0, i_L = GV_P\}\end{aligned} \tag{4}$$

where V_P is a non-zero solution of v_1 from

$$i_M(v_1, x) = (G_N - G)\, v_1 \tag{5}$$

It is worth noting that P_0 always exists, but P_+ and P_- only exist if the nonlinear part exhibits an active conductance. This necessary condition can be formally written as

$$G_M(0, x) < G_N - G \tag{6}$$

The oscillation patterns born from a Hopf bifurcation that we seek to generate can be characterized via some conditions on the eigenvalues of the Jacobian matrix J evaluated at each EP. At P_0, J must have a unique real positive eigenvalue,

while the others have a negative real part (condition *i*). Instead, J evaluated at P_+ and P_- must show a complex conjugate pair of eigenvalues with a positive real part, being the other eigenvalue real negative (condition *ii*). Designing the tunable memristor Chua's circuit with such conditions on the eigenvalues is necessary to guarantee the oscillation patterns we are targeting. While finding expressions for the impedances and nonlinear part parameters that satisfy all the conditions on the eigenvalues is possible, it requires complex analysis of the circuit bifurcations, already explored in detail for different nonlinearities in [27] and [28]. Our approach is to simplify such exploration by making some choices based on results reported in previous works.

From [27], we know that choosing certain values for Chua's circuit adimensional parameters α and β defined as

$$\alpha = \frac{C_2}{C_1}, \quad \beta = \frac{C_2}{G^2 L} \tag{7}$$

guarantee the eigenvalues conditions at P_0 (condition *i*), as long as (6) is also satisfied (details about Chua's circuit adimensional equations can be found in [27]). For instance, this is true with $\alpha = 10$ and $\beta = 14$, which are chosen for this work unless otherwise stated. In order to select G_N, we can refer to [29], where the instability at P_0 is forced by imposing that the trace of J vanishes when evaluated at P_0, which ensures that the sum of the real part of the eigenvalues is null and thus implying that P_0 is unstable. This condition leads to a convenient relationship between G_N and G_M

$$G_N = G_M(0, x) + G\left(1 + \alpha^{-1}\right) \tag{8}$$

It can be verified that condition (8) implies (6) and, by arguing as in the appendix of [29], that condition *i* is satisfied.

Moreover, [27] also reports the condition for a Hopf bifurcation to occur, or equivalently the starting point at which condition *ii* for P_+ and P_- is satisfied. The circuit design must be valid for a range of memristor states characterized by a differential conductance value evaluated in V_P, i.e., $G_M(V_P, x)$. Condition *ii* results in boundary values for $G_M(V_P, x)$, which we name G_H and which are defined as

$$\beta = -\alpha \frac{G_H - G_N}{G}\left(1 + \alpha + \alpha \frac{G_H - G_N}{G}\right) \tag{9}$$

Equation (9) is a second-order equation for G_H, whose solutions are

$$G_{H,i} = G_N - \frac{G}{2\alpha}\left(1 + \alpha \pm \sqrt{(1+\alpha)^2 - 4\beta}\right), \quad i = 1, 2 \tag{10}$$

and thus there exist only if

$$(1+\alpha)^2 - 4\beta > 0 \tag{11}$$

Both solutions constitute an upper and lower bound for $G_M(V_P, x)$ in which the eigenvalue condition *ii* for P_+ and P_- is guaranteed. This interval is

$$G_{H,1} < G_M(V_P, x) < G_{H,2} \tag{12}$$

It is worth noting that the existence of Hopf bifurcations is guaranteed for the previously chosen $\alpha = 10$ and $\beta = 14$ since they satisfy (11).

Furthermore, an additional design constraint considered for the tunable memristor Chua's circuit is the need to contain the v_1 voltage span of the trajectory inside the memristor non-switching region to avoid that x changes in the oscillation mode. Since it is not possible to determine analytically the v_1 voltage span of chaotic trajectories, we opted for a heuristic approach based on numerical simulations. After evaluating multiple trajectories, we observed that the maximum v_1 is proportional to the first coordinate V_P of the EPs P_+ and P_-, also noticed in the trajectories of Fig. 1(d). This observation can be translated in the form of the boundary as

$$\max(v_1) \leq k \cdot V_P \tag{13}$$

Here, k depends on the employed nonlinear part and can be determined by numerical simulations. From this finding, using (13) to limit v_1 voltage span implies fixing the positions of EPs P_+ and P_-, thus forcing G to a specific value, according to (6).

Concluding, the tunable memristor Chua's circuit can operate as a programmable oscillator if the conditions from (6), (11) and (12) are simultaneously satisfied, i.e., the three EPs in (4) exist, P_0 is unstable, and both P_+ and P_- undergo to a Hopf bifurcation along a valid range of x values. Additionally, the trajectory amplitude can be modulated through the EPs coordinates to meet the memristive device specifications. However, these guidelines must be complemented with the specific nonlinearity of the memristive device to be included in order to complete the tunable memristor Chua's circuit design.

III. Physical Implementation and Experimental Verification

A. RRAM Device Switching Operation

In this work, we use resistive random-access memory (RRAM) devices consisting of 50 nm Pt/5.5 nm HfO_2/40 nm TiN stacks with a 40×40 μm^2 area. Their fabrication process is reported in detail in [30] and [31]. Electrical measurements have been performed using a B1500 Keysight semiconductor parameter analyzer in voltage-controlled mode while reading the current passing through the device. The voltage is always applied at the top Pt electrode, keeping the TiN electrode grounded.

The RRAM device requires an electroforming process in order to show resistive switching properties, which is carried out by applying a negative voltage and limited by a current compliance to avoid the device breakdown (not shown, -3 V with a 1 mA limit). Once electroformed, the device remains in a low resistive state (LRS). Fig. 2(a) shows a typical bipolar resistive switching cycle exhibited by the device. Starting from the LRS, a RESET operation gradually programs the device to a high resistive state (HRS) by applying a positive voltage (in the example, 2 V). Conversely, a SET operation abruptly drives the device from the HRS back to the LRS by applying a negative voltage and current compliance; the voltage at which the SET event takes place is called SET voltage (V_{SET}). Here LRS and HRS are qualitative terms to refer to the RRAM device state after a SET or a RESET operation, respectively. The internal state x of our device can be tuned in an analog

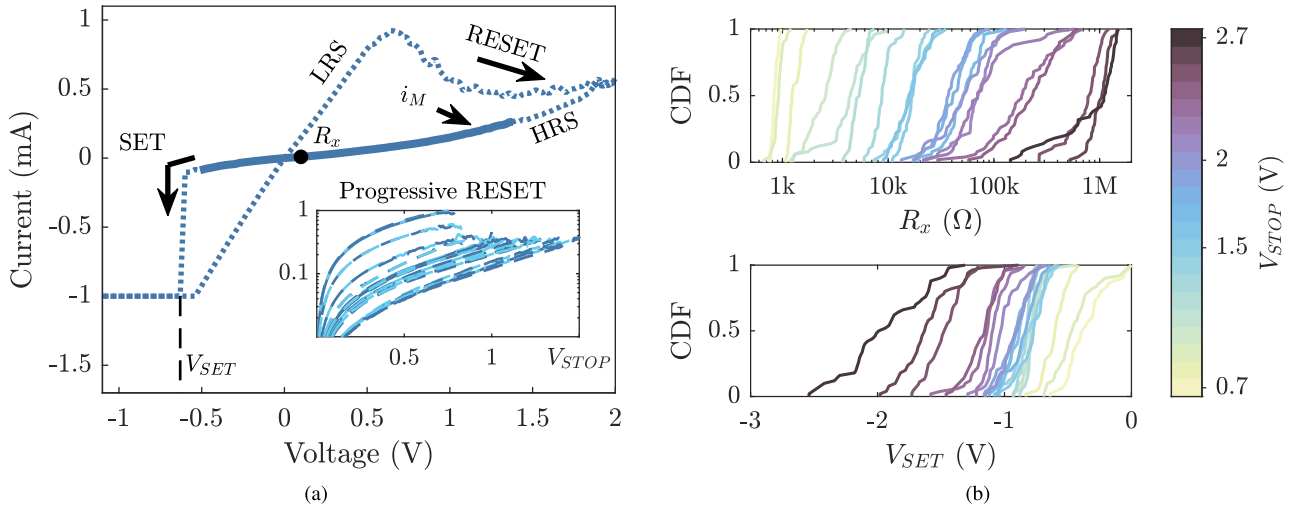

Fig. 2. RRAM device switching operation. (a) Illustration of a single switching cycle and extracted features from the programmed HRS. Inset: example of a progressive RESET programming procedure with $V_{STOP} = 1.5$ V. (b) Cumulative distribution functions of V_{SET} and R_x according to the V_{STOP} in the RESET programming procedure.

fashion and it is monitored through R_x, which is the sensed resistance at 0.1 V, as shown in Fig. 2(a). The state retention of our devices has been measured to extend up to 10 years [31], [32].

The switching cycle in Fig. 2(a) highlights the HRS nonlinear i-v characteristics (thick continuous line) in contrast with the high linearity in the LRS. Therefore, implementing the nonlinear part of Fig. 1(a) requires our RRAM device to be programmed to a HRS. As we must avoid switching the RRAM device during the programming mode, we need to identify the device non-switching region. The exact non-switching region may be a topic of discussion since it is not a fixed region and it may depend on the time in which a voltage is applied across the device. Generally, RRAM devices switch at lower voltages if these voltages are applied for longer times [33], [34]. Since our circuit oscillates at least at a moderate frequency, we accept the SET and RESET voltages acquired in our quasi-static measurements as valid references. Therefore, we can consider the device non-switching region at voltages between V_{SET} and the maximum voltage applied in the RESET operation (thick line labeled as i_M in Fig. 2(a)).

B. Phenomenological Model of i_M

The nonlinear current $i_M(v, x)$ from the RRAM device HRS is characterized and modeled to be used in the tunable memristor Chua's circuit, shown in Fig. 1(a). The model considers the nonlinearity of i_M and accounts for the internal state x of the RRAM device in the form of R_x.

The electrical characterization of the i_M at different HRS is carried out employing a programming procedure referred to as progressive RESET and shown in the inset of Fig. 2(a). Starting from similar initial LRS conditions by employing the same SET operation as in Fig. 2(a), a sequence of RESET operations is carried out. More specifically, the first RESET operation applies 0.7 V, and for each following RESET operation the voltage increases by 50 mV, until reaching a target value we refer to as stop voltage or V_{STOP}. At this point, the RRAM device is programmed to a HRS. This method is preferred to avoid excessive stress in some switching events and possible device breakdowns, especially when switching from LRS to HRS with voltage levels higher than the ones used in previous works [31]. Both the last RESET operation at each progressive RESET procedure and a subsequent SET operation are used to extract i_M, R_x and V_{SET} from the programmed HRS.

The HRS electrical characterization data set consists of acquired i_M, R_x and V_{SET} from 50 progressive RESET procedures for each V_{STOP} starting from 0.7 V to 2.7 V. Fig. 2(b) reports the experimental cumulative distribution functions (CDF) for R_x and V_{SET} according to each employed V_{STOP}. When V_{STOP} increases, R_x generally increases, while V_{SET} becomes more negative, and as a result, the device non-switching region increases. It is worth noticing that the well-known cycle-to-cycle (C2C) variability of RRAM devices is present in the progressive RESET programming and manifested in the depicted CDFs. For instance, the reported distributions for both R_x and V_{SET} tend to partially overlap when using progressive RESET procedures with closer V_{STOP} values. Additionally, the spread of values significantly increases at higher V_{STOP}. Despite the uncertainty after the programming, the collected data with a broad distribution of R_x values are exploited to establish a model linking R_x with the i-v characteristics from the HRS.

The proposed model for the i_M exhibited at the HRS is presented in (14); it corresponds to a third-order polynomial nonlinearity with respect to the voltage drop across the RRAM device, and it considers the possibility of an asymmetric i_M according to the applied voltage polarity. The model contains four coefficients, p_{1p}, p_{3p}, p_{1n} and p_{3n}, for the linear and third-order terms, and for both positive and negative voltage polarities. Given the fact that i_M is monotonically increasing as shown in Fig. 2(a), the coefficients are restricted to positive values. Moreover, different HRSs result in different i-v curves and different values for the model coefficients. For this reason, we consider the model coefficients to depend on the state estimator R_x.

$$i_M(v, R_x) = \begin{cases} p_{1p}(R_x)v + p_{3p}(R_x)v^3, & v \geq 0 \\ p_{1n}(R_x)v + p_{3n}(R_x)v^3, & v < 0 \end{cases} \tag{14}$$

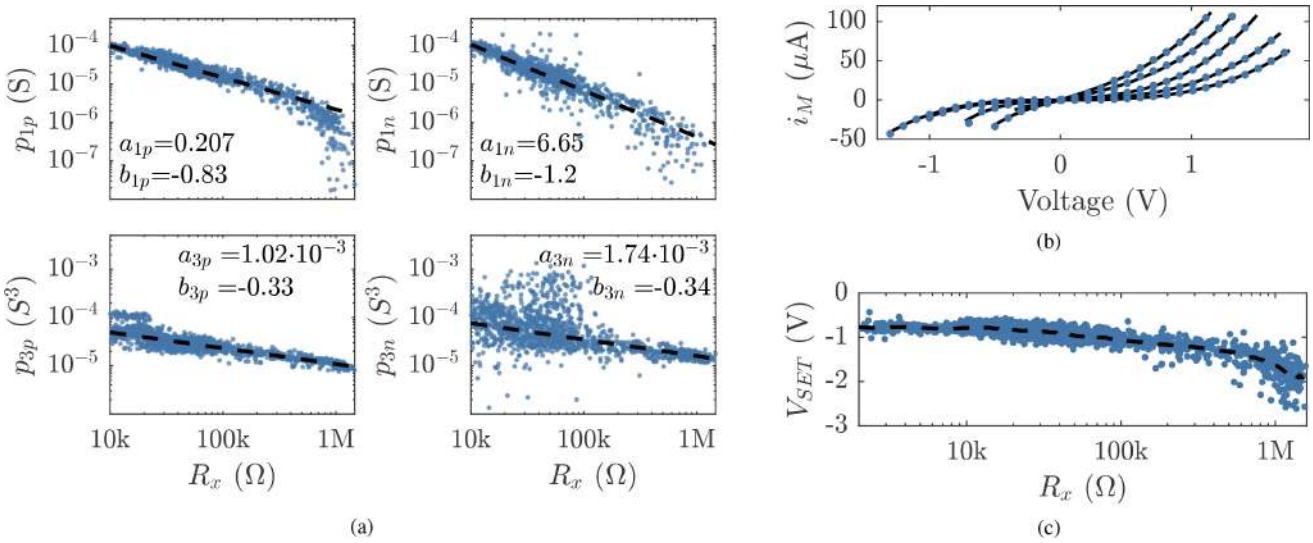

Fig. 3. Results of the fitting process for the current measurements with the model proposed in (16). (a) Model coefficients from (14) after fitting each i_M versus R_x and exponential law trend from (15). (b) Examples of measured i_M data (dots) and fitted model (line). (c) V_{SET} dependence with R_x (average trend depicted in dashed line).

Fig. 3(a) displays the results of the model coefficients after fitting each acquired i_M individually according to the R_x of that programmed HRS, while Fig. 3(b) illustrates with few examples how the model properly fits the experimental data. From Fig. 3(a), it is noticeable that all coefficients are related to R_x, each one approximately following a power law relationship, described as

$$p_i(R_x) \approx a_i R_x^{b_i} \tag{15}$$

This fact demonstrates that R_x is a good measure of the internal state x, at least on average. Moreover, a certain internal state is associated with a certain average nonlinearity (given by the third-order term coefficient).

Combining (14) and (15), we obtain the following model for i_M that explicitly depends on the tunable and measurable R_x

$$i_M(v, R_x) = \begin{cases} \left[a_{1p} R_x^{b_{1p}}\right] v + \left[a_{3p} R_x^{b_{3p}}\right] v^3, & v \geq 0 \\ \left[a_{1n} R_x^{b_{1n}}\right] v + \left[a_{3n} R_x^{b_{3n}}\right] v^3, & v < 0 \end{cases} \tag{16}$$

Fig. 3(a) depicts the estimation of each coefficient p_i using (15) as a black dashed line and reports the parameter values for each estimation. The estimation of each p_i highlights the nonlinear nature of HRS; as R_x increases, p_1 (linear term) decreases at a higher rate than the p_3 (cubic term). Furthermore, for each polarity, both the depicted estimations and the parameters of (16), i.e., the pairs a_{ip}-a_{in} and b_{ip}-b_{in} (for $i = 1, 3$), show differences and suggest certain asymmetry in the overall i-v characteristics. It is most notable when comparing the first-order coefficients p_{1p} and p_{1n} at the highest R_x, where the difference is almost one order of magnitude. However, third-order coefficients p_{3p} and p_{3n} are very similar and at least an order of magnitude higher than p_{1p} and p_{1n}. Therefore, the asymmetry is largely mitigated in the total current at moderate voltages; at very low voltages, however, the first-order term dominates and some asymmetry is assumed. Apart from the asymmetry, it is also worth pointing out the deviation of some coefficients p_i with the estimation from (15). The source for this uncertainty can be attributed to the fact that we are condensing the internal state x of the RRAM device into the single magnitude R_x and the coefficients p_i have dependencies with multiple state variables. Nevertheless, R_x constitutes a good measure of x on average.

Summarizing, the model in (16) predicts the current of the programmed RRAM device just by sensing R_x. It is worth noting the improvement with respect to our preliminary work [23], where polynomial even terms used to model the asymmetry showed poor correlation with R_x. It is critical to remind that the validity of the model is limited to the voltages in which the measured i_M is used for fitting, i.e., voltages below V_{STOP} and V_{SET}. Based on Fig. 2(b), $|V_{SET}| < V_{STOP}$ is generally true. Since the v_1 voltage span from our Chua's circuit is considered to be symmetric with respect to the origin, V_{SET} constitutes a more restrictive boundary. Fig. 3(c) displays the measured V_{SET} at each programmed HRS and as a function of R_x. The average trend, shown in a dashed line, will be used as a reference for limiting the v_1 voltage span in the circuit implementation.

C. Circuit Design, Implementation and Experimental Setup

The design guidelines exposed in Section II-B are adapted to our RRAM device characteristics to implement our tunable version of Chua's circuit. Prior to applying them, we need to specify the working region for our RRAM device. We prioritized operating the RRAM device at a higher R_x since it allows us to safely operate at higher v_1 values during the circuit's oscillation mode. For instance, we chose the region of $R_x \in [0.1, 1]$ MΩ, expecting to operate at voltages between ±1.2 V, according to the expected V_{SET} in Fig. 3(c). Working with lower R_x would restrict the oscillation mode to voltages down to 0.5 V, which is too low for implementations with discrete components.

For the sake of design, we consider a specific state $\tilde{x}$ around which to design the circuit and identify it by the value $\widetilde{R_x}$.

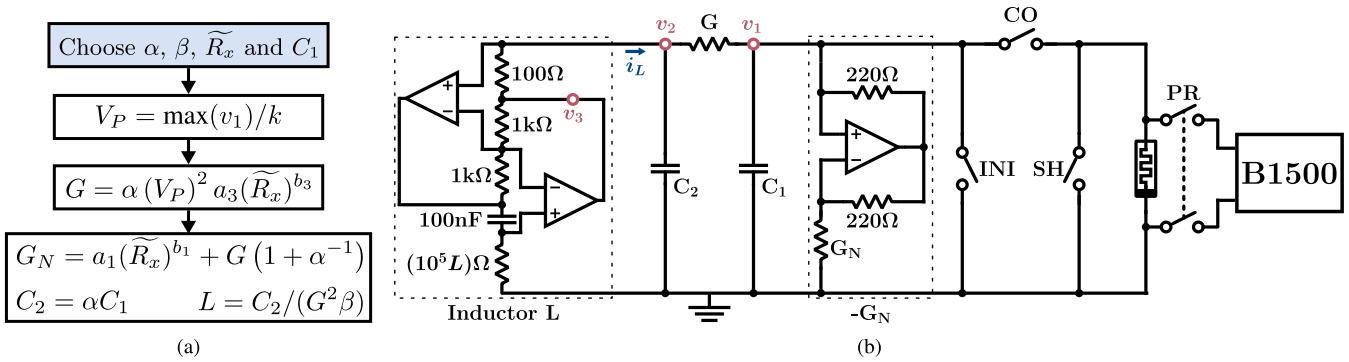

Fig. 4. Physical implementation of the tunable memristor Chua's circuit. (a) Workflow of the circuit design. (b) Scheme of the physical implementation. Oscilloscope probes acquire the circuit trajectory by measuring voltages v_1, v_2, and v_3.

We use the model for the device HRS current from (16) to find expressions for G_N and G that explicitly depend on $\widetilde{R_x}$. More specifically, (5) and (8) are combined with (16), resulting in

$$G_N = a_1(\widetilde{R_x})^{b_1} + G\left(1+\alpha^{-1}\right) \tag{17}$$

$$G = \alpha\,(V_P)^2\, a_3(\widetilde{R_x})^{b_3} \tag{18}$$

With these new expressions and previous considerations from Section II-B, the tunable Chua's circuit is designed using the workflow depicted in Fig. 4(a). The design procedure allows few choices; unless otherwise specified, we use $\alpha = 10$, $\beta = 14$, $C_1 = 10$ nF and $\widetilde{R_x} = 500$ kΩ. Regarding the calculation of V_P, we determined with simulations that, for the nonlinearity exhibited in (16), $k = 1.33$.

The complete setup for the experimental validation is shown in Fig. 4(b). It comprises Chua's circuit and the semiconductor analyzer for programming the device. The circuit elements are implemented on a breadboard except for the RRAM device, which is connected to the rest of the circuit through a probe station.

The implemented circuit presents additional elements with respect to the circuit from Fig. 1(a). The operational amplifier (OPAMP) configuration in the middle of Fig. 4(b) implements the negative conductance $-G_N$ as long as the OPAMP operates in the linear region. The feedback resistors are chosen at a value low enough to guarantee the OPAMP linear region for a v_1 voltage span considerably larger than the expected values during the oscillation mode. Besides, a low offset voltage OPAMP like AD743 is required to minimize non-idealities in the nonlinear part.

Furthermore, the inductance is emulated with a gyrator circuit [35] with relatively few components. It saves circuit area, especially for high inductances, and the inductance can be conveniently modified just by changing the bottom resistor value. Moreover, it allows us to indirectly acquire i_L by sensing the voltages v_2 and v_3 in Fig. 4(b).

Finally, four switches with different functionalities are also added. The programming (PR) switch is used to shift between programming (closed position) and oscillation (open position) modes. The other switches were included as additional protection measures to address issues we encountered in our experimental setup. The connection (CO) switch avoids interferences between the semiconductor parameter analyzer sensing circuitry and the rest of Chua's circuit during the programming mode. We also found that the RRAM device RS was sensitive to mechanical manipulations during the connection to Chua's circuit; the shunt (SH) switch protects the RRAM device during the connection process. Lastly, the initialization (INI) switch introduces an initial condition for Chua's circuit ($v_1 = 0$) and prevents the negative conductance circuit from saturating, which would bring v_1 to either of the OPAMP supply voltages and potentially harm the RRAM device. We want to emphasize that only the switch PR is strictly required and that the other switches can be omitted in an integrated circuit design.

The experimental procedure for testing the tunable Chua's circuit is carried out as follows. Initially, the RRAM device is programmed to a HRS using a progressive RESET procedure; the R_x value of the HRS is also acquired in the process. Once programmed, the RRAM device is connected to the rest of Chua's circuit. After this, Chua's circuit autonomously starts to oscillate and the voltages v_1, v_2, and v_3 are acquired using a digital oscilloscope MSO6430.

D. Circuit Experimental Verification

The circuit is tested in two different scenarios. The first one involves tuning the inductance L rather than the RRAM device R_x, to demonstrate that the nonlinearity from the RRAM device is suitable to generate multiple trajectories. The second scenario corresponds to the original purpose of the circuit, i.e., tuning trajectories by programming the RRAM device into different resistance states.

In the first experience, the tunable memristor Chua's circuit is designed around an already programmed RRAM device. The design procedure is used to select the circuit impedances (details in Fig. 5). A set of inductance values $L = \{700, 660, 580\}$ mH is chosen, which corresponds to $\beta = \{14, 15, 17\}$. The three components allow us to obtain the trajectories depicted in Fig. 5, namely the symmetric aperiodic (Fig. 5(a)), the asymmetric aperiodic (Fig. 5(b)), and the asymmetric periodic (Fig. 5(c)). For each case, the state space representation and the temporal evolution of v_1, v_2, and i_L are reported. The aperiodic nature of chaotic patterns can be appreciated in the trajectories from Fig. 5(a) and 5(d), and from Fig. 5(b) and 5(e), especially from the symmetric aperiodic trajectory, where the trajectory arbitrarily switches from orbiting around the EPs P_+ to P_-. The v_1 coordinate for EPs P_+ and P_- seems to be placed close to ± 0.8 V, similar

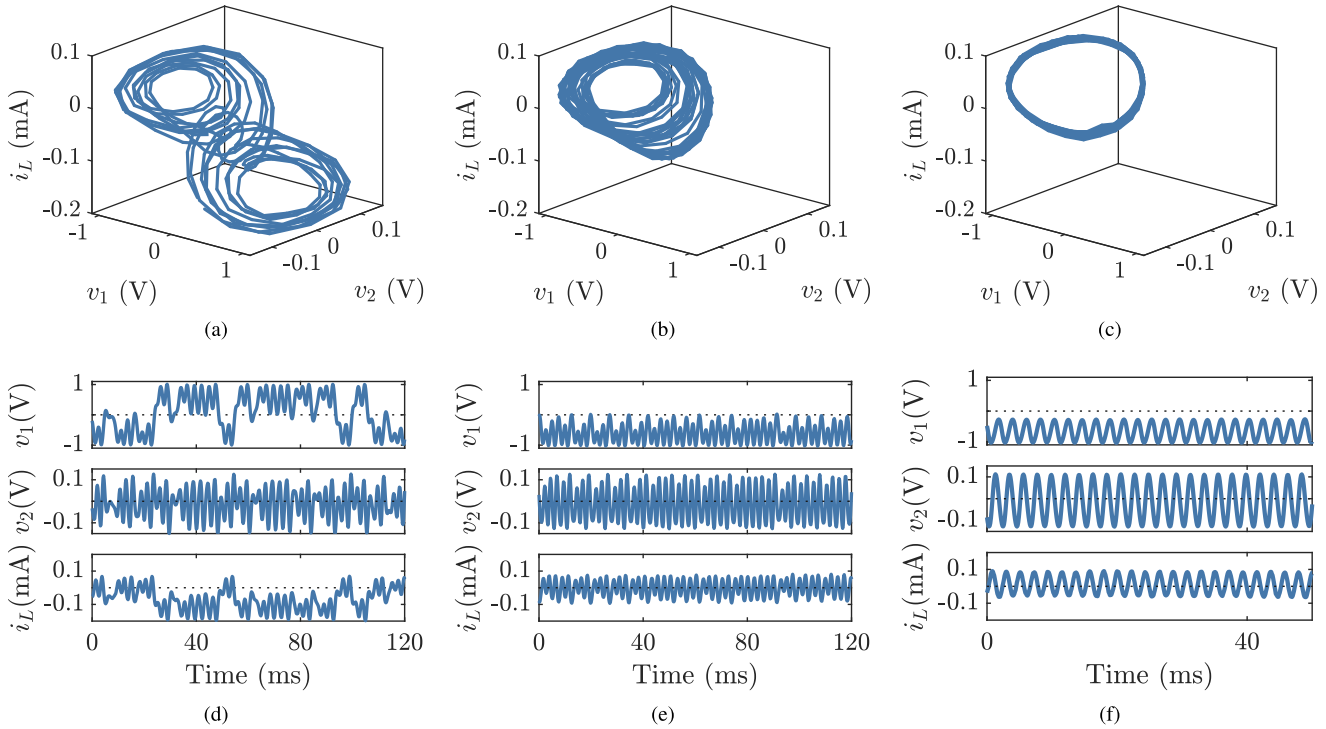

Fig. 5. Tunable memristor Chua's circuit experimental trajectories with RRAM devices programmed to fixed $\widetilde{R_x} = 664$ kΩ while modifying L. Other impedances are set to $G = 100$ μS (10 kΩ), $G_N = 114$ μS (8.8 kΩ), $C_1 = 10$ nF and $C_2 = 100$ nF. (a)-(c) State space representation and (d)-(f) temporal evolution of the state variables of symmetric aperiodic ($L = 700$ mH), asymmetric aperiodic ($L = 660$ mH) and asymmetric periodic ($L = 580$ mH) trajectories, respectively.

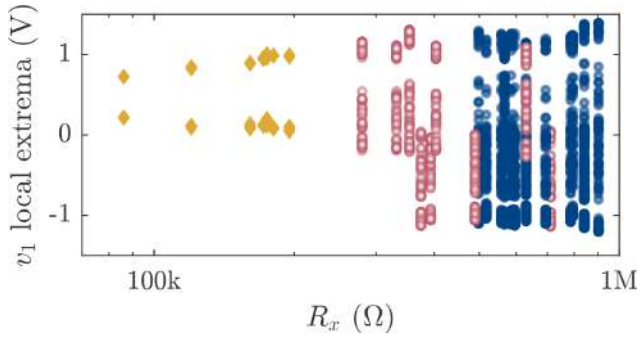

Fig. 6. Experimental bifurcation diagram with R_x as a bifurcation parameter, displaying asymmetric periodic (yellow diamonds), asymmetric aperiodic (red empty circles) and symmetric aperiodic (blue filled circles) trajectories. Modified from [23].

to the $V_{P+} = 0.9$ V aimed at the design. It is worth noticing that the EPs do not change since all the components related to the EPs position (defined by (5)), i.e., G and the nonlinear part, are kept fixed.

In the second experiment, the inductance is kept fixed at $L = 567$ mH, while the RRAM device is programmed to different resistive states. For each programmed resistive state, the local extrema of the v_1 as a function of R_x are displayed in the bifurcation diagram of Fig. 6. This representation is enough to understand if a trajectory is symmetric or not (with respect to $v_1 = 0$ V) and aperiodic or periodic (if the local extrema are spread along a dense cloud of points or condensed in limited positions). We were able to tune the circuit to generate different trajectories. For instance, there are examples of asymmetric periodic, asymmetric aperiodic, and symmetric aperiodic trajectories, depicted with diamond-shaped, empty circle, and filled circle markers, respectively.

The results of the bifurcation diagram raise some interesting observations. The different oscillation patterns appear as R_x increases, transitioning from asymmetric periodic trajectories to aperiodic or chaotic ones. This transition corresponds to the period-doubling route of chaos. Similarly to oscillation patterns, the v_1 voltage span generally increases with R_x since the EPs P_+ and P_- move away from the origin. These trends highlight the role of the state estimator R_x as a tunable parameter for the tunable memristor Chua's circuit. However, this general evolution is not completely uniform. For instance, some asymmetric and symmetric aperiodic trajectories are overlapped in the region $R_x \in [0.5, 1)$ MΩ, and the v_1 voltage span sometimes fluctuates with similar R_x. We believe that the most plausible explanation for these nonidealities is related to the fact that we are using R_x as an estimator of the internal state x. The i-v characteristic and its nonlinearity are determined by R_x only on average. This means that variations in the device internal state may result in variations in the nonlinearity even at equal R_x, which is translated into a certain deviation with respect to a uniform trend in the bifurcation diagram. Nevertheless, the reported results were already very promising, considering that devices were not optimized specifically for the proposed application.

IV. Discussion Regarding Desirable Device Characteristics

The experimental results prove the possibility of implementing the tunable memristor Chua's circuit with our RRAM device. However, the bifurcation diagram in Fig. 6 is only possible after designing the circuit aiming to a specific R_x range, and the trajectory selection by V_{STOP} is limited due

to C2C variability. This section discusses which memristor characteristics can potentially improve the tuning possibilities of our Chua's circuit. All the findings in this section are supported by numerical simulations using our model for i_M in (16).

The memristor non-switching region is the first obstacle we found toward a robust tunable memristor Chua's circuit realization. It has already been pointed out how SET and RESET voltages limit the v_1 voltage span during the oscillation mode. Therefore, the most desirable attributes for the non-switching region are the following: (1) symmetric SET and RESET voltages to optimize the allocation of the symmetric Chua's circuit trajectories, and (2) a reasonable voltage span (± 1 to 1.5 V) can be applied across most of their RS without switching the memristor.

C2C variability is the second most important issue to account for. In our experimental attempt, just a few different V_{STOP} values can be used to tune the memristor resistive state, and in some cases, these voltages are not able to select the same kind of trajectory repetitively. The cause is the high variability in R_x, as shown in Fig. 3(c). A device with narrow R_x distributions, e.g., $\pm 10\%$ of the expected R_x, may mitigate this problem. Alternatively, the use of program & verify procedures reduce the impact of C2C variability [36].

In addition to these device features, the characteristics of the nonlinear current i_M also play an important role in the circuit response. Particularly, two different aspects are identified: the overall current level and the nonlinear deviation of i_N. We define nonlinear deviation as the memristor current deviation from its linear term. For our i_M model, it can be easily quantified since the nonlinear and linear terms are separated. To evaluate the influence of both these aspects on the tunable memristor Chua's circuit performance, we introduce two scaling factors at eq. (14), resulting in

$$i_M(v, R_x) = \begin{cases} s_L \left[p_{1p} v + s_D \cdot p_{3p} v^3 \right], & v \geq 0 \\ s_L \left[p_{1n} v + s_D \cdot p_{3n} v^3 \right], & v < 0 \end{cases} \tag{19}$$

Here, s_D and s_L are the nonlinear deviation and current level scaling factors, respectively. Briefly, when the value of these scaling factors increases, the contribution of the nonlinear term and the overall current level of i_M also increase. The particular case $s_D = s_L = 1$ refers to our device.

We first comment on the effect of the current level (s_D kept at 1). When the overall current level in i_M decreases, i.e.,s_L decreases, the oscillation patterns do not change significantly after using the workflow in Fig. 4(a). However, the design workflow scales down the dissipative loads G and G_N to match the i_M parameters. This results in two noticeable changes in the circuit trajectory: i_L current level decreases and the trajectory evolves at a faster pace. This in turn scales down the total power consumption with s_L. For instance, using the default choices in the design workflow, decreasing s_L from 1 to 0.1 scales down the total power consumption by an order of magnitude, from 230 μW to 24 μW. Therefore, devices with the possibility of exhibiting lower current levels than our device can become key for low-power solutions.

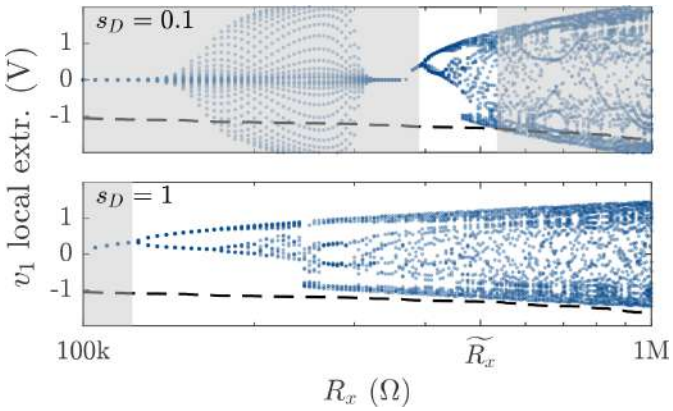

Fig. 7. Simulation results of the tunable memristor Chua's circuit showcasing two nonlinear deviations: $s_D = 0.1$ (top) and $s_D = 1$ (our device, bottom). Mean V_{SET} across R_x from Fig. 3(c) (dashed line). Shaded areas depict regions out of the valid range of R_x values for tuning.

Next, we discuss the impact of the nonlinear deviation (s_L kept at 1). As mentioned before, nonlinear i_M is mandatory for this circuit in order to exhibit different oscillations, including chaos. It is beneficial, if not critical, that the i_M shape shows a high enough nonlinear deviation. Fig. 7 depicts two bifurcation diagrams obtained through numerical simulations using the default choices in the design workflow and two different s_D values of 0.1 (top) and 1 (our device, bottom). The dashed line depicts the average trend V_{SET} from Fig. 3(c), while the shaded areas depict forbidden values of R_x for tuning. Comparing both bifurcation diagrams, a higher nonlinear deviation ($s_D = 1$) stretches the bifurcation diagram; this also occurs when evaluating other s_D. The stretching increases the range of R_x in which the circuit can be tuned. The range of valid R_x values in the bifurcation diagrams in Fig. 7 is limited due to two different factors. The lower limit of the R_x is due to the Hopf bifurcation (condition *ii* is not fulfilled). For $s_D = 0.1$, it occurs around 400 kΩ, while in $s_D = 1$, it is enlarged up to 130 kΩ. However, an upper limit of 535 kΩ appears only when $s_D = 0.1$, since the rapid increase of the v_1 envelope does not adequately fit within the device V_{SET}. In conclusion, larger nonlinear deviations allow the circuit to be tuned to a wider range of R_x, which otherwise would be very limited (as seen for $s_D = 0.1$) and probably not practical due to C2C variability.

V. Conclusion

A physical implementation of the tunable memristor Chua's circuit based on a RRAM device has been presented. Our circuit benefits from the RRAM device integration in two ways: (1) a more compact nonlinear part after incorporating nonlinear i-v characteristics to produce chaotic oscillations, and (2) revealing bifurcations by tuning the resistive state in the RRAM device. In order to exploit these properties, the i-v characteristics and switching properties of a RRAM device are characterized and modeled, emphasizing their dependence on the resistive state. At the same time, circuit design guidelines targeting circuit oscillations and guaranteeing safe operation voltages for the RRAM are provided. Finally, the experimental verification of the tunable memristor Chua's circuit validates

both the proposed model for the RRAM device i-v characteristics and the design methods.

The proposed framework for the tunable memristor Chua's circuit is not limited to RRAM devices and can be employed with other nonvolatile memristive devices, such as phase-change memories. Anyhow, we identified three device properties that may become critical for a successful implementation. First, symmetric resistive switching events located at voltages high enough are desirable to have room for tuning between different oscillation patterns. Second, high C2C variability hinders repeatability from aiming for identical circuit trajectories. Finally, the higher nonlinear characteristics may be critical for the device to become a useful tunable element inside the circuit.

The tunable memristor nonlinear block implemented in this work can be included in other circuits that admit similar nonlinearities. This way, nonvolatile memristive devices can open the path to offering a compact solution to different oscillators for controlling the generation of chaos, useful in cryptography or sensing applications. But more importantly, we expect that the tunability feature is not limited to a mere oscillation pattern selector. Instead, when considering tunable nonlinear oscillators as a primitive of more complex computing architectures, such as oscillator-based computing or reservoir computing, the nonvolatile memristive device can play the role of a "tuning knob" to improve the overall computing performance.

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